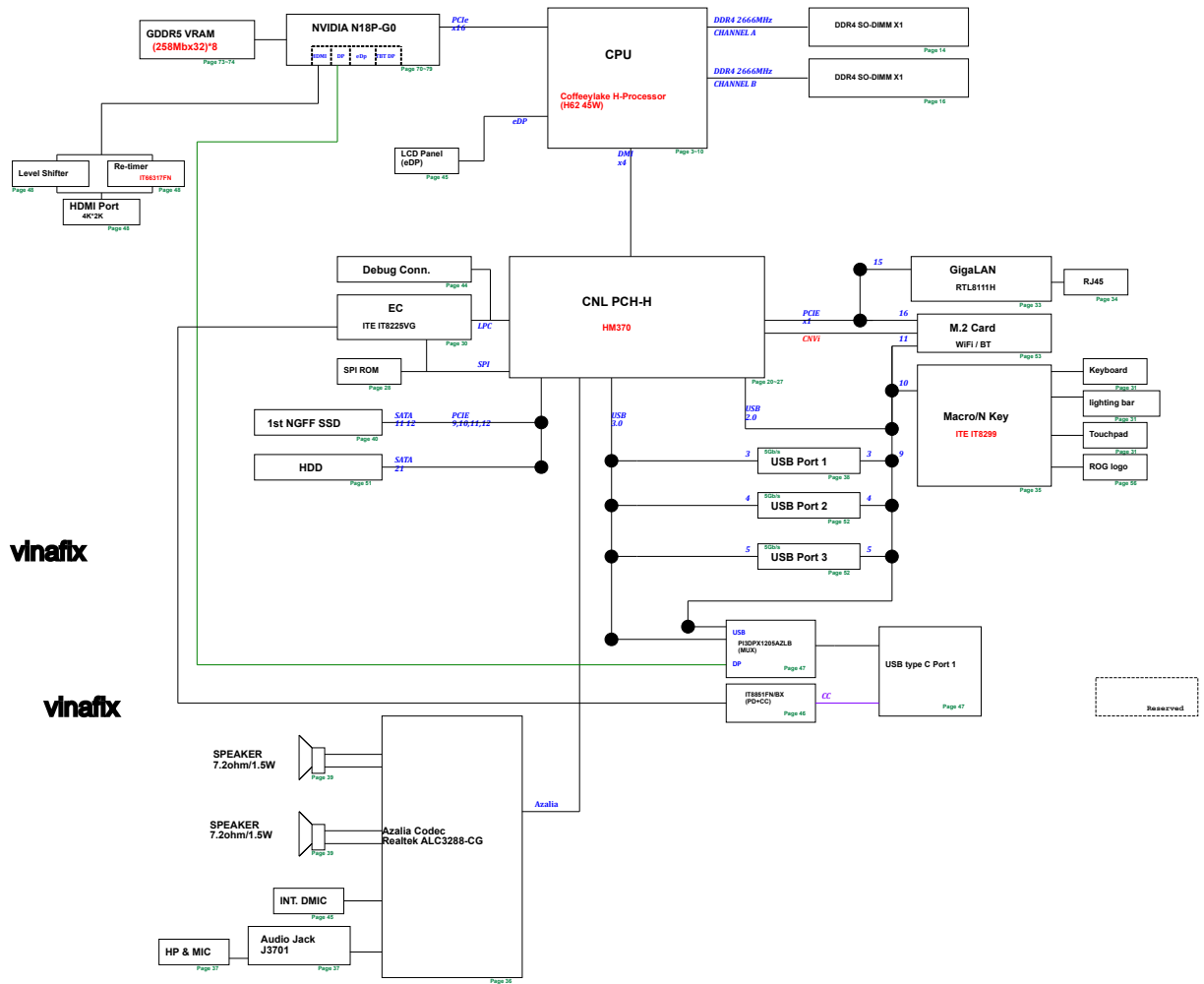


001_Block Diagram
002_System Setting
003_CPU_DMI,PEG,eDP,DDI
004_CPU_DDR4
005_CPU_GND
006_CPU_CFG,RSVD
007_
008_CPU_PWR
009_CPU_PWR
010_CPU_POWER_CAP
011_TBT_Alpine-Ridge
012_TBT_TPS65982&Type C
013_TBT_PWR
014_DIM_DDR4 SO-DIMM A(0)
015_DIM_DDR4 SO-DIMM B(0)
016_DIM_DDR4 SO-DIMM A(1)
017_DIM_DDR4 SO-DIMM B(1)
018_DIM_CA/DQ Voltage
020_PCH_HOA,SMB,SEQ,RTC,JTAG
021_PCH_POE,SATA,USB2,MISC
022_PCH_CLK,LPC,USB3
023_PCH_LVDS,eDP,DP
024_PCH_SPI,CNV
025_PCH_GPIO
026_PCH_POWER,GND
027_PCH_POWER,GND
028_PCH_SPI ROM,OTH
029_TEST_POINT
030_KBC_IT2225
031_KBC_KB & TP
032_RST_Reset Circuit
033_LAN_RTL8111H-CG
034_LAN_RJ45_CON
035_MacroN_KEY_IT25291
036_AUD_ALC295
037_AUD_EXT Jack
039_AUD_INT SPK
040_NGFF_SSD_PCIE_CON
041_NGFF_SSD_PCIE_CON_3
042_CR_GL3215
043_
044_BUG_LPC
045_eDP_CON & Tobii IS4_CON
046_
047_Display Port
048_HDMI
049_
050_FAN_Thermal Sensor & Fan
051_HDD
052_USB3.0 Port
053_NGFF_WLAN & BT & XBOX
055_USB3.0 Port
056_LED & Switch
057_DSG_Discharge
058_Power Protect
059_EMI
060_DC & BAT IN
063_>>>Power Button_JO_BD
064_>>>LED_IO_BD
065_ME_W2B conn. & NUT
066_
067_
068_
069_
070_GPU_PCIE I/F
071_GPU_POWER
072_GPU_FRAME BUFFER
073_VRAM-CHANNEL A
074_VRAM-CHANNEL B
075_VRAM-CHANNEL C
076_VRAM-CHANNEL D
077_VRAM_CAP
080_PW_COFFEE LAKE (1)
081_PW_COFFEE LAKE (2)
082_PW_VCCIO
083_PW_+1.05VSUS
084_PW_+1.8VSUS
086_PW_+1.2V/+VTT/+2.5V
087_PW_+3VADSW/+VSUS
088_PW_LOAD SWITCH
089_PW_CHARGER
090_PW_PROTECTION
091_PW_+NVVDD (1)
092_PW_+NVVDD (2)
093_PW_+NVVDD5
094_PW_+FBVDDQ
096_PW_+12VS_FAN
097_PW_PEX_VDD
098_PW_IPC
100_Power On Timing-AC mode
101_Power On Timing-DC mode

G531GT Block Diagram

Coffeelake H Platform



vinaftx

- Reset Circuit
- Thermal Sensor
- PWM Fan
- Switch & LEDs
- Discharge Circuit
- Power Protect
- DC & Battery
- Skew Holes

Power

+VCCORE+VCCSA+VCCGT

+VCCIO

+1.05VSUS

+1.8VSUS

1.2V/+VTT/2.5V

+3VADSW/+VSUS

Load Switch

Charger

Protection

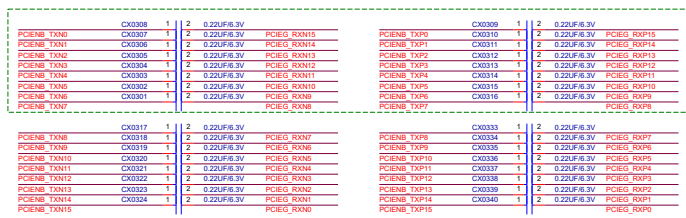
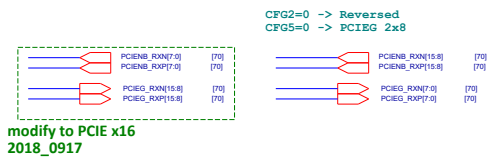
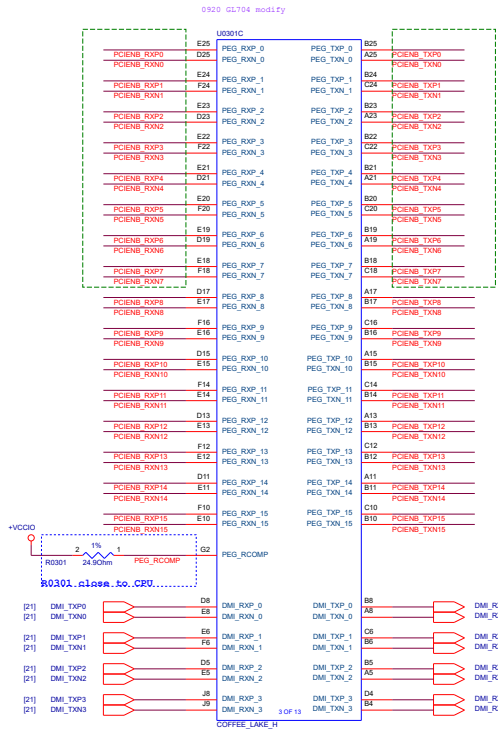
VGA CORE (+NVVDD)

+NVVDD5

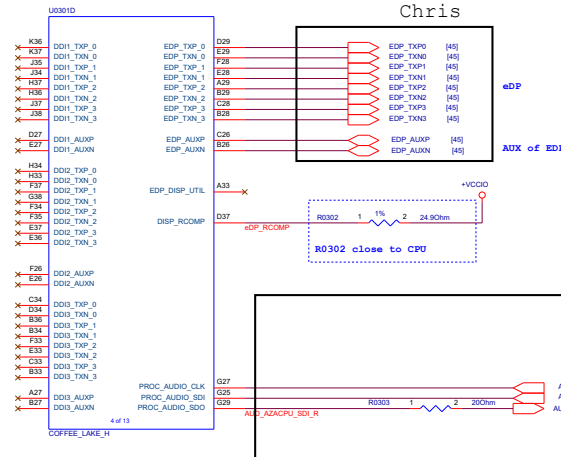
+FBVDDQ (+1.55V)

IPC

PCIE6



Display



Chris

Table 8-3. Few Supported Normal and Lane-reversed Bifurcation Configurations

x16 Controller Negotiated Width	x8 Controller Negotiated Width	x4 Controller Negotiated Width	Processor	Physical Lanes											
				0	1	2	3	4	5	6	7	8	9	10	11
x16	Off	Off	Direct	0	1	2	3	4	5	6	7	8	9	10	11
x8	x8	Off	Direct	0	1	2	3	4	5	6	7	0	1	2	3
x8	x4	x4	Direct	0	1	2	3	4	5	6	7	0	1	2	3
x16	Off	Off	Reverse	15	14	13	12	11	10	9	8	7	6	5	4
x8	x8	Off	Reverse	7	6	5	4	3	2	1	0	7	6	5	4
x8	x4	x4	Reverse	3	2	1	0	3	2	1	0	7	6	5	4

Notes:

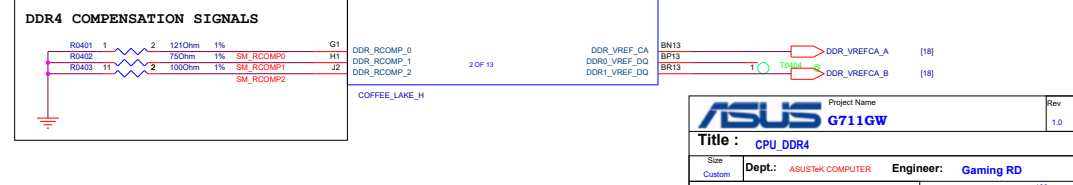
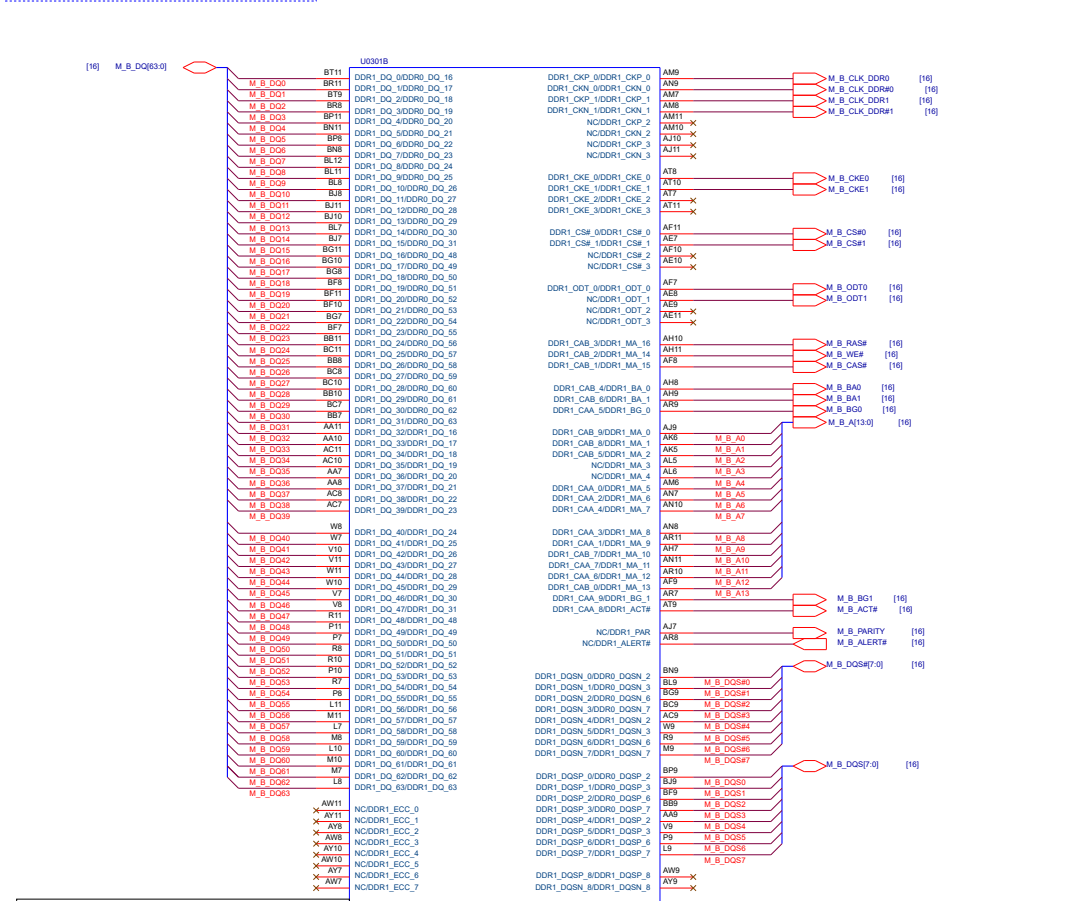
- Support is also provided for narrow width and use devices with lower number of lanes (that is, usage on x4 configuration), however further bifurcation is not supported.
- In case that more than one device is connected, the device with the highest lane count, should always be connected to the lower lanes, as follows:
 - Connect lane 0 of 1st device to lane 0.
 - Connect lane 0 of 2nd device to lane 8.
 - Connect lane 0 of 3rd device to lane 12.For example:
 - a. When using 1x8 + 2x4, the 8 lane device must use lanes 0:7.
 - b. When using 1x4 + 1x2, the 4 lane device must use lanes 0:3, and other 2 lanes device must use lanes 8:9.
 - c. When using 1x4 + 1x2 + 1x1, 4 lane device must use lanes 0:3, two lane device must use lanes 8:9, one lane device must use lane 12.

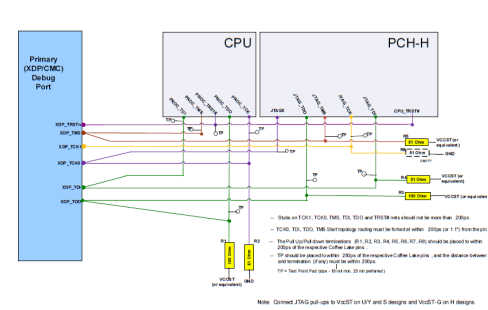
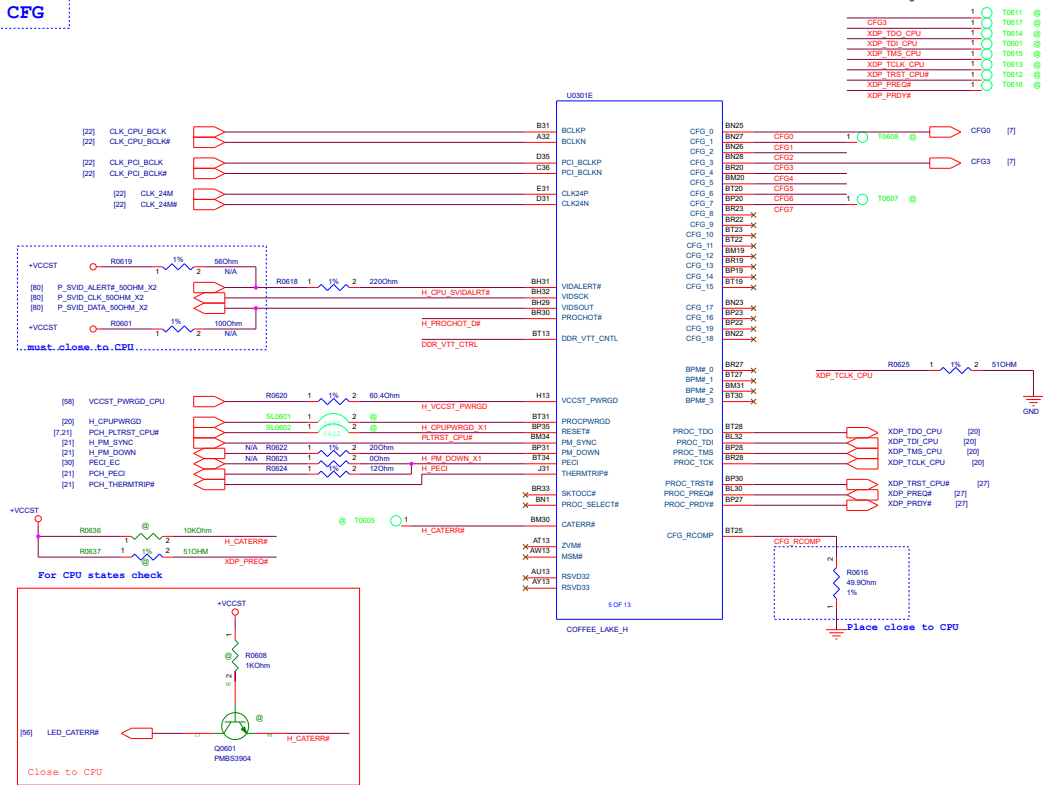
31.1.4 Disabling and Termination Guidelines for the Intel® High Definition Audio Interface

When HDA_SDIN[1:0], DISPA_SDIN interface is not implemented on the platform the signal pin(s) may be left unconnected.

When the Intel® Display Audio interface is not implemented, PROC_AUDIO_CLK and PROC_AUDIO_SDI need to be terminated to GND via a weak pull-down resistor (i.e. ~2KΩ), PROC_AUDIO_SDO can be left unconnected.

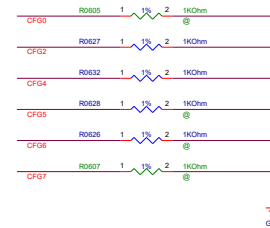
Main Board





Chris

CFG Straps



CFG Straps for Processor

ref : Intel 570805_Coffeelake_EDS_Vol_1_Rev1.4 P.121

CFG[0] : Stall reset sequence after PCU PLL lock until de-asserted
--

- 1 : (Default) Normal Operation; No stall

CFG[1] : Reserved Configuration Lane

Reserved Configuration Lane

CFG[2] : PCI Express® Static x16 Lane Numbering Reversal

- 1 : (Default) Normal Operation
- 0 : Lane Numbers Reversed

CFG[3] : Reserved configuration lanes

Reserved Configuration Lane

CFG[4] : eDP Enable

- 1 : Disabled
- 0 : Enabled

CFG[6:5] : PCI Express® Bifurcation

- 00 : 1 x8 , 2 x4 PCI Express*
- 01 : Reserved
- 10 : 2 x8 PCI Express*
- 11 : 1 x16 PCI Express*

CFG[7] : PEG Training

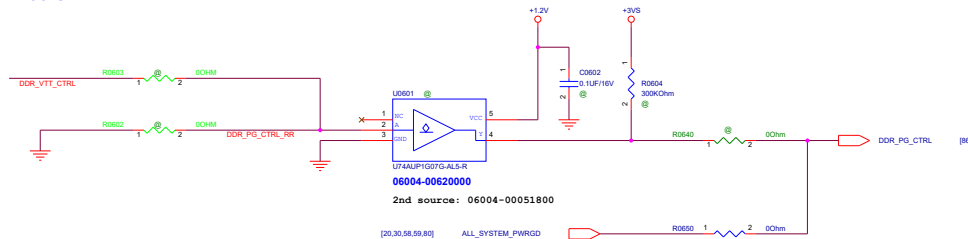
- 1 : (Default) PEG Train Immediately Following RESET# de-assertion
- 0 : PEG Wait for BIOS for Training

CFG[19:8] : Reserved Configuration Lanes

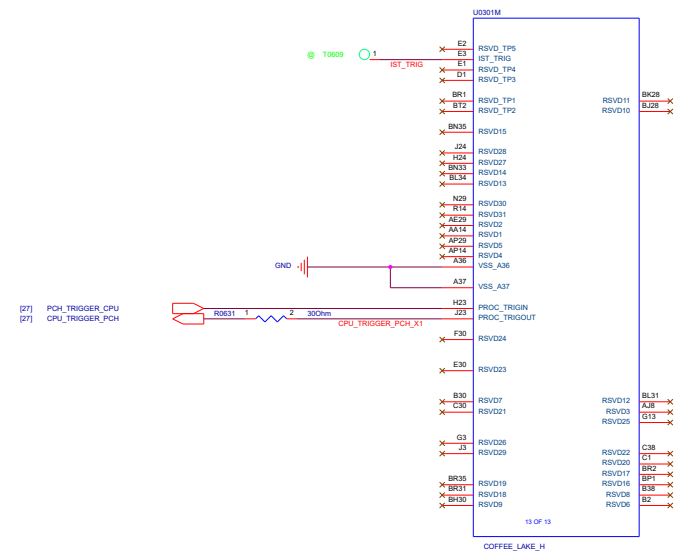
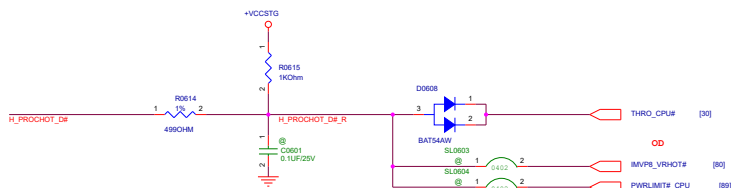
Reserved Configuration Lanes

DDR VTT CTRL:
System Memory Power Gate Control:
Disables the platform memory VTT regulator
in C8 and deeper and S3.
Ref: Intel 570805_Coffeelake_EDS_Vol_1_Rev1.5 P.116

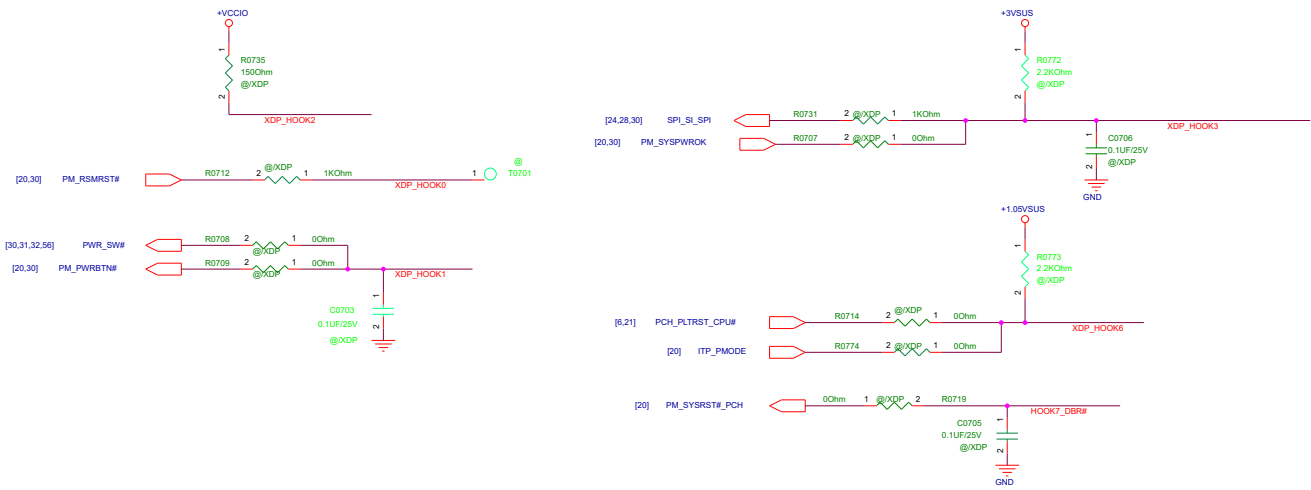
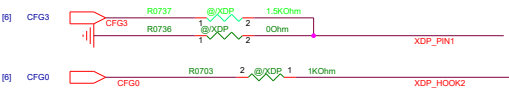
VTT Enable

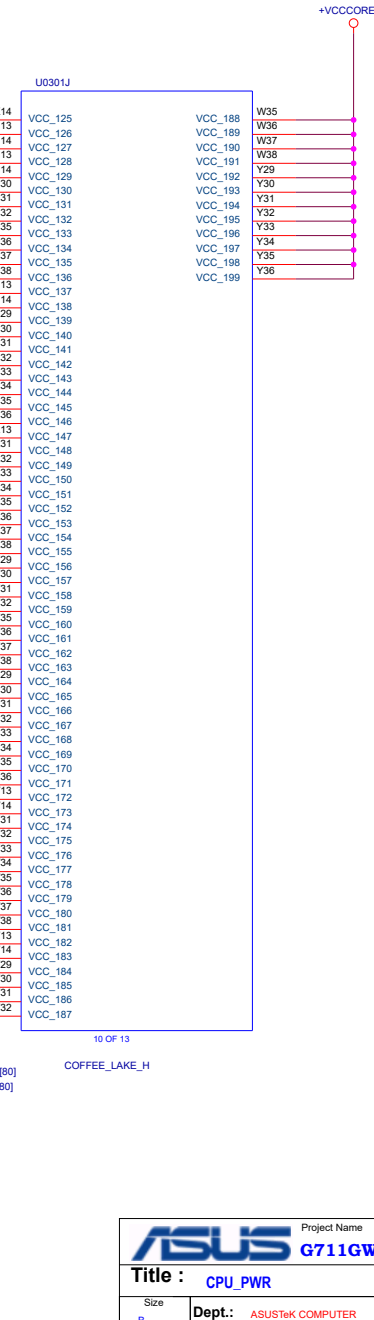
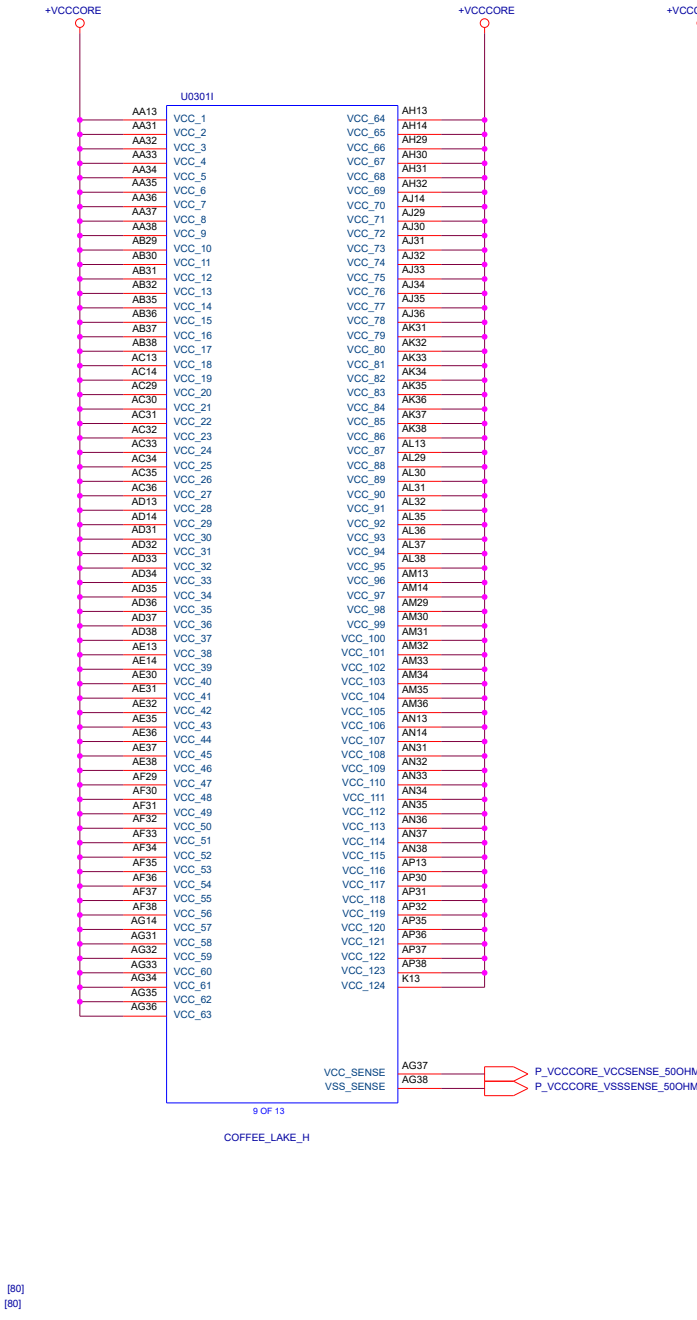
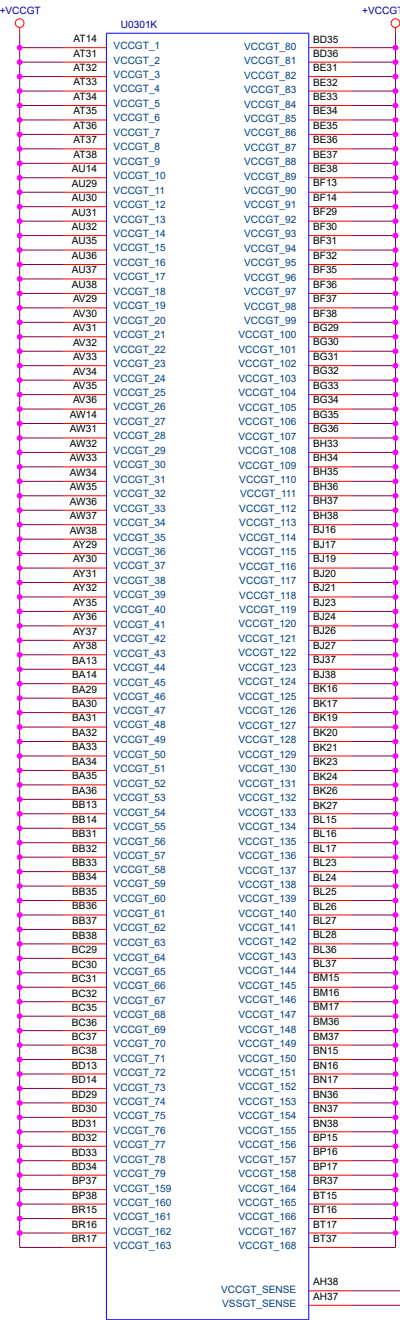


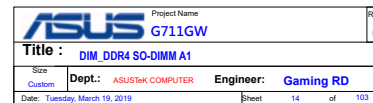
CPU SIDEBAND SIGNALS



CPU XDP







SODIMM CHB-DIMM0 TOP H4.0mm STD (J1601)

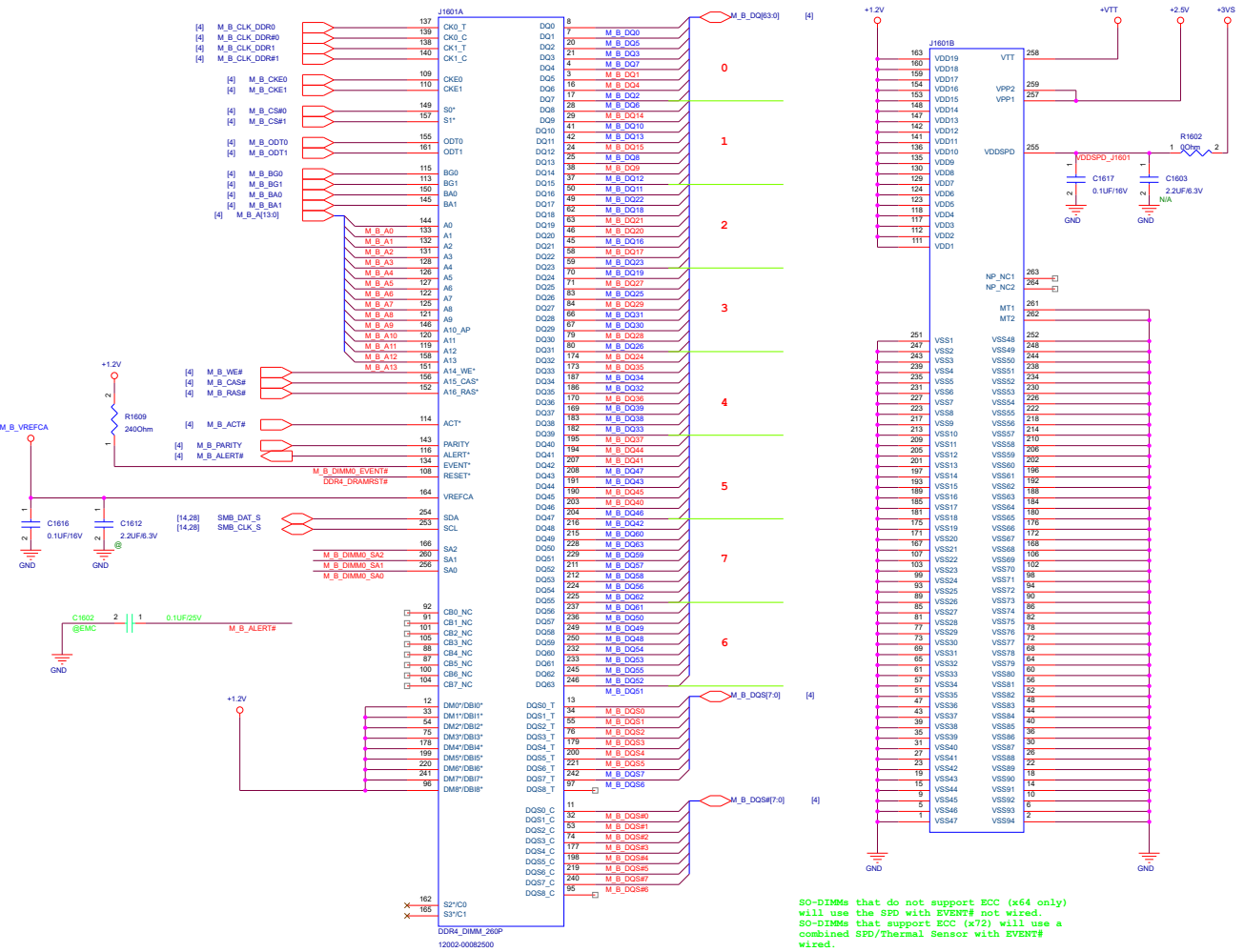
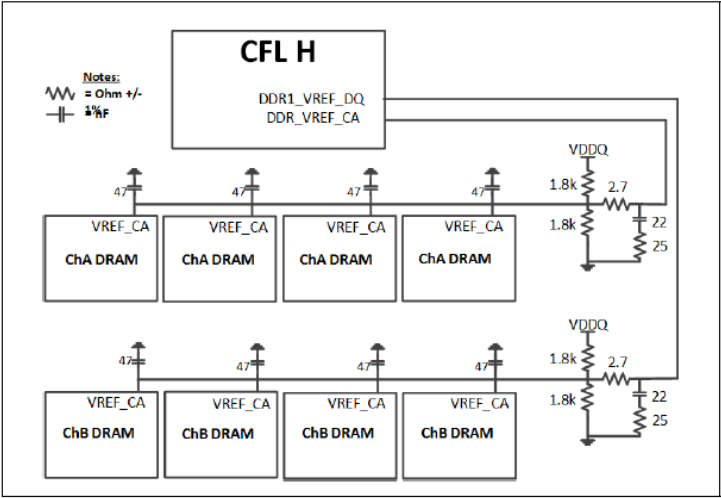


Figure 4-23. CFL H DDR4 x16 Memory Down V_{REF-CA} Overview



Vref for CHA_DIMM0

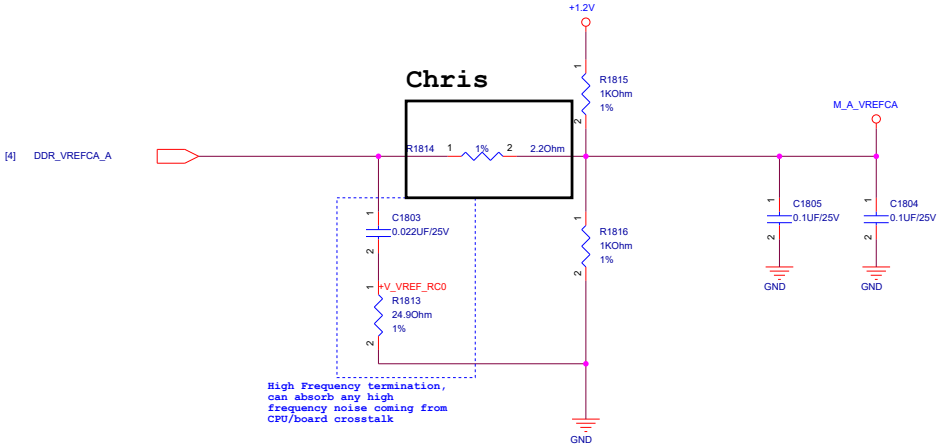
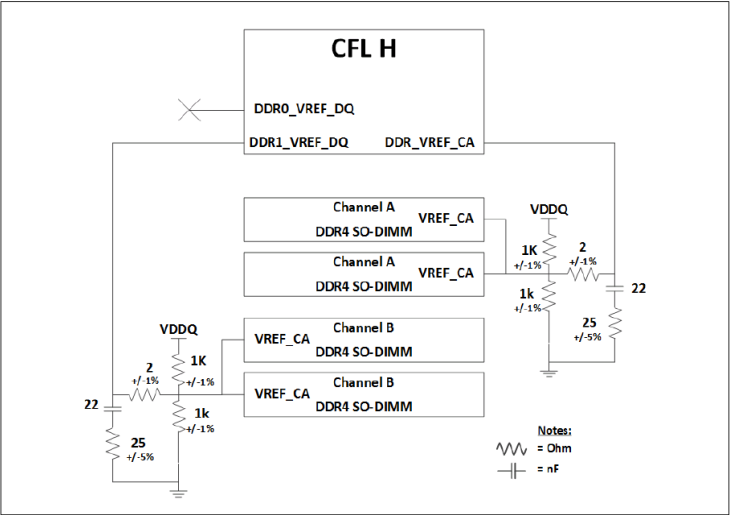
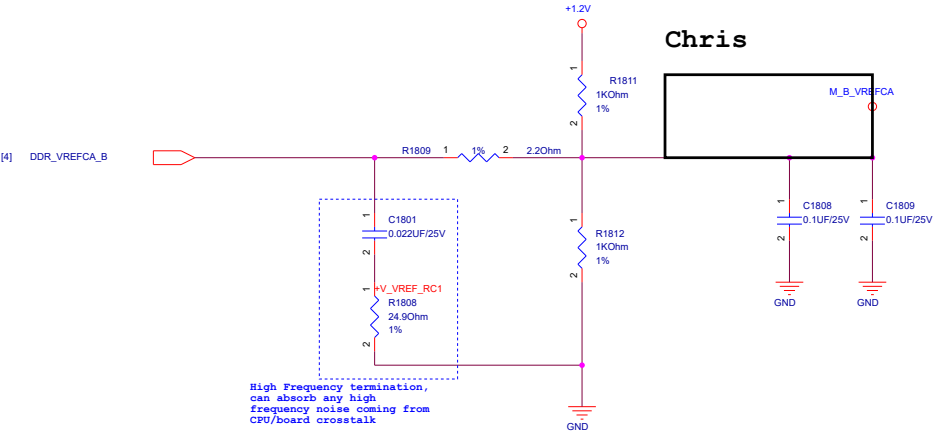


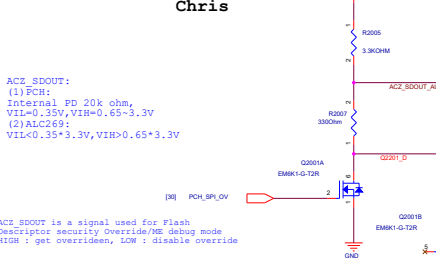
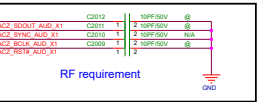
Figure 4-22. CFL-H DDR4 SO-DIMM V_{REF-CA} Overview



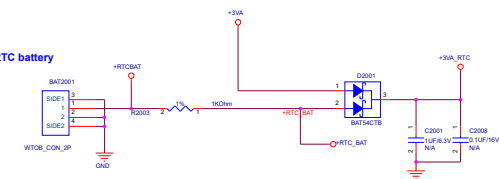
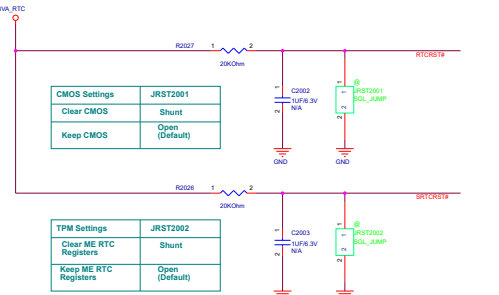
Vref for CHB_DIMM0



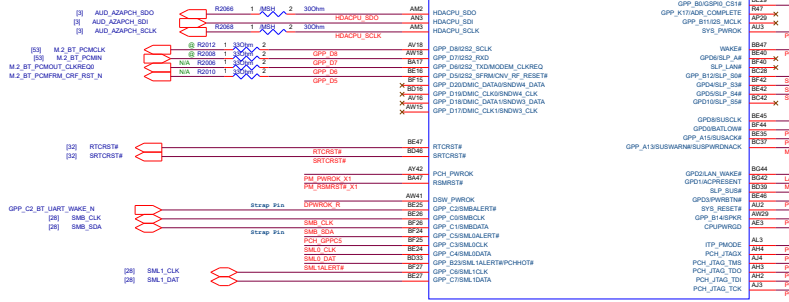
HD Audio



Main Source	1th PWR	2nd PWR	3rd PWR	4th
+RTCBAT	+RTC_BAT	+3VA_RTC		
	+1.05VSD	+VCCST		
	+1.2V			
AC_BAT_SYS	+3VAO	+3VA	+3VA_EC	
	+3VA_DSW	+3VSD	+3VSD_PCH	+V3_3A_V1_3A_VCCP2D0
		+3VS		

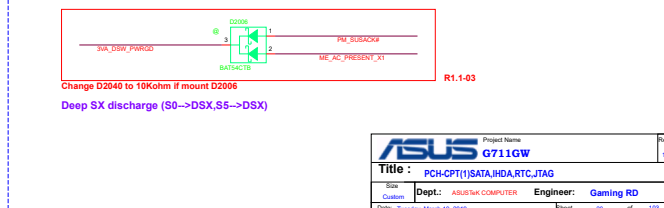
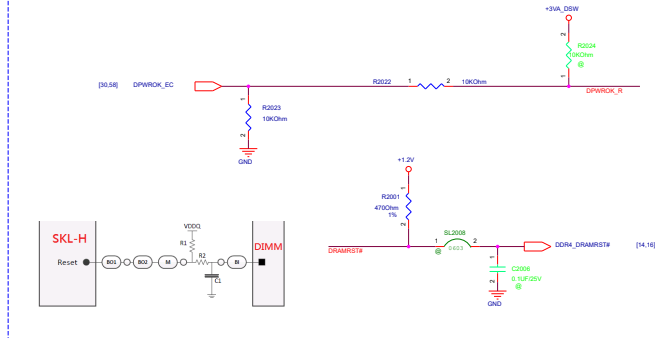
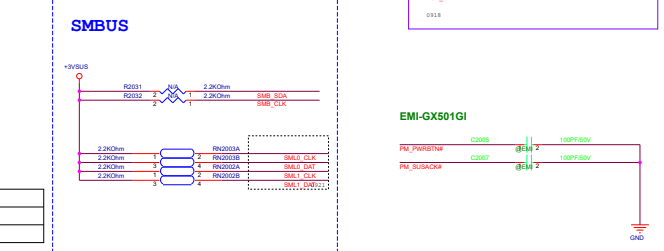
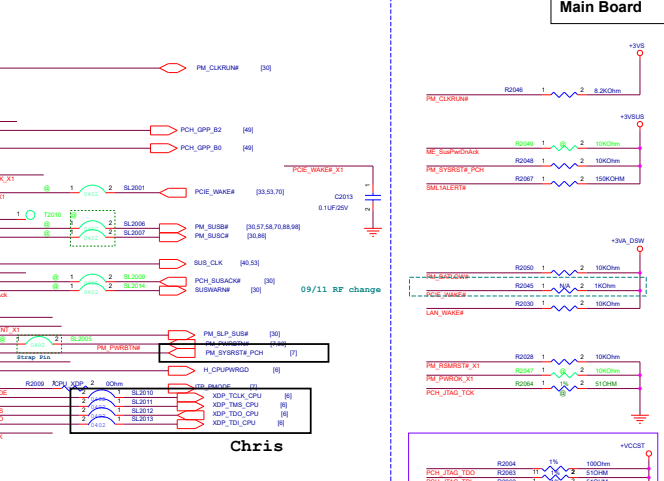
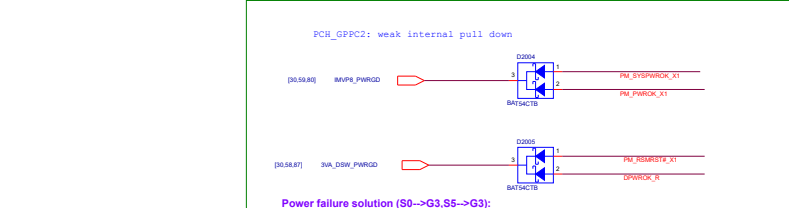
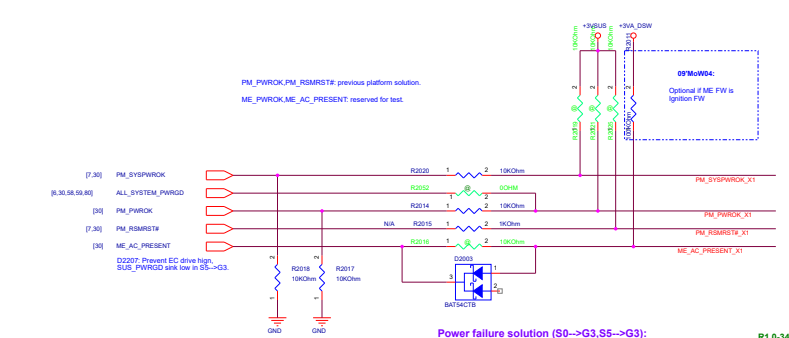


1st :12017-00020200
2nd :12027100002C
USE RTC Battery:
PIN: 0B100-00040500 BATT-LI CR1220 3V



Power failure solution (S0-->G3,S5-->G3):

eSPI or LPC		TIS Confidentiality		Top Swap Override	
PU	eSPI	PU	Enable	PU	Enable
PD	LPC (default)	PD	Disable (default)	PD	Disable (default)



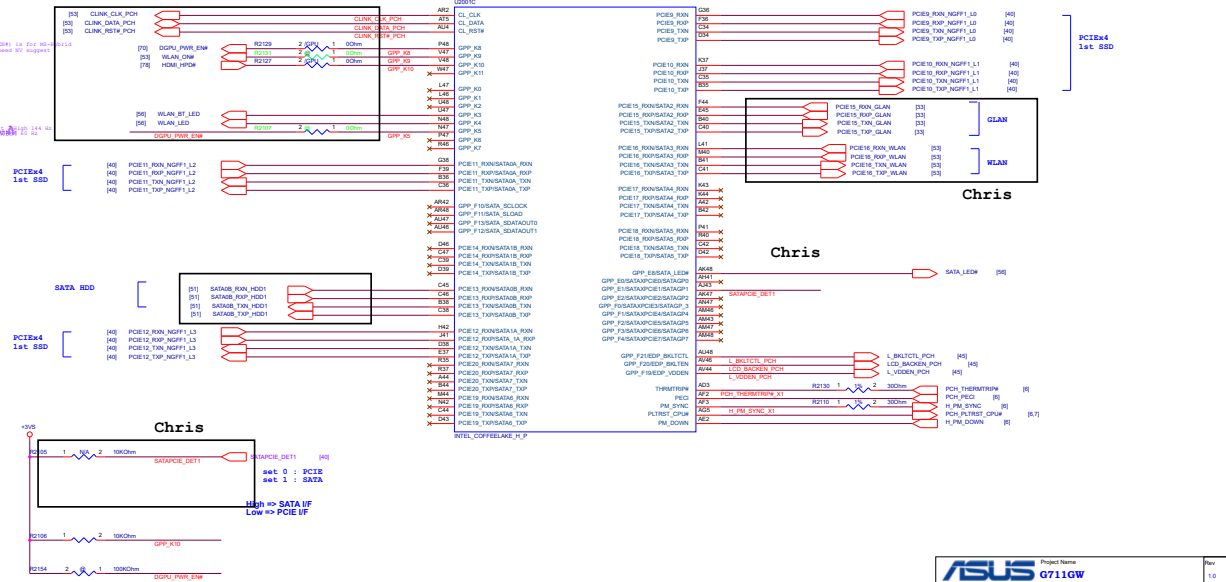
Main Board

1610 Conclusion	Remark
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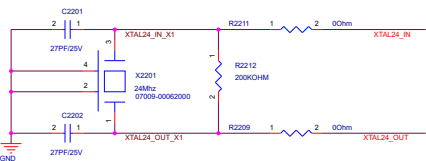
	Function
CLKREQ-0	GPU
CLKREQ-1	
CLKREQ-2	CR
CLKREQ-3	WLAN
CLKREQ-4	
CLKREQ-5	TBT AR
CLKREQ-6	PCIe SSD
CLKREQ-7	
CLKREQ-8	
CLKREQ-9	
CLKREQ-10~15	



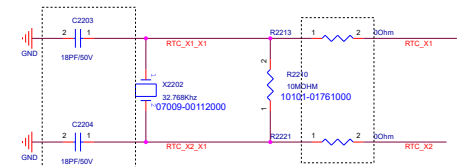
teknisi indonesia



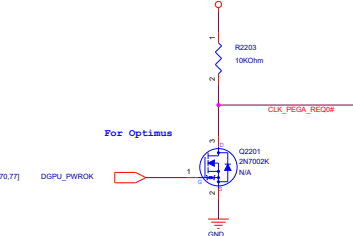
XTAL 24MHz



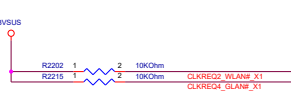
RTC CRYSTAL 32.768KHz



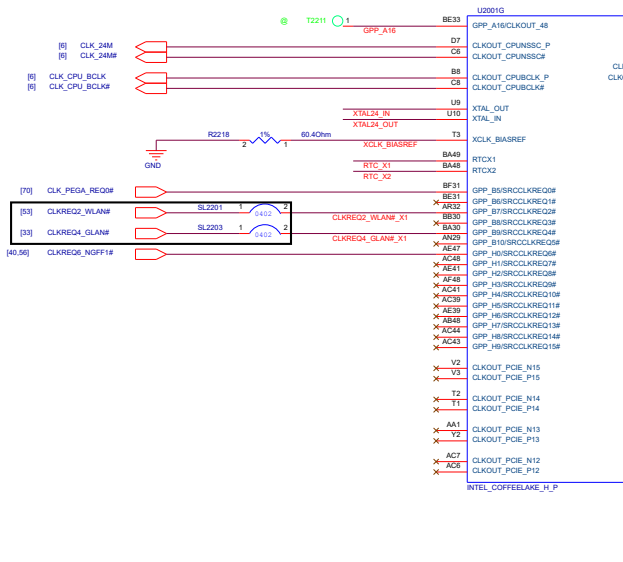
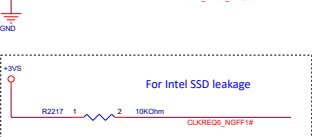
DGPU CLKReq#



PCH CLKREQ Setting:



For Intel SSD leakage



MB USB3.0 : NIA

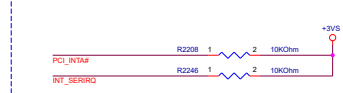
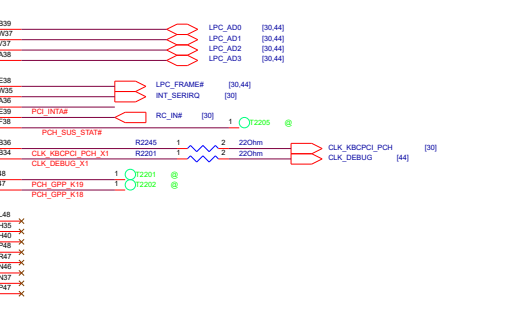
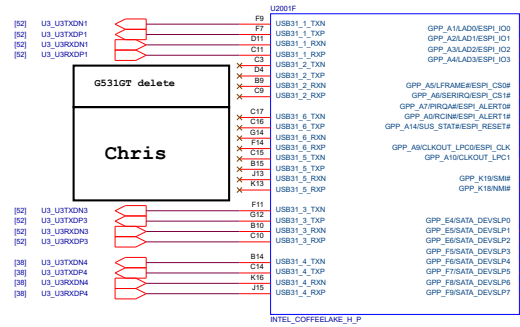
USB3.0 Type C : Left

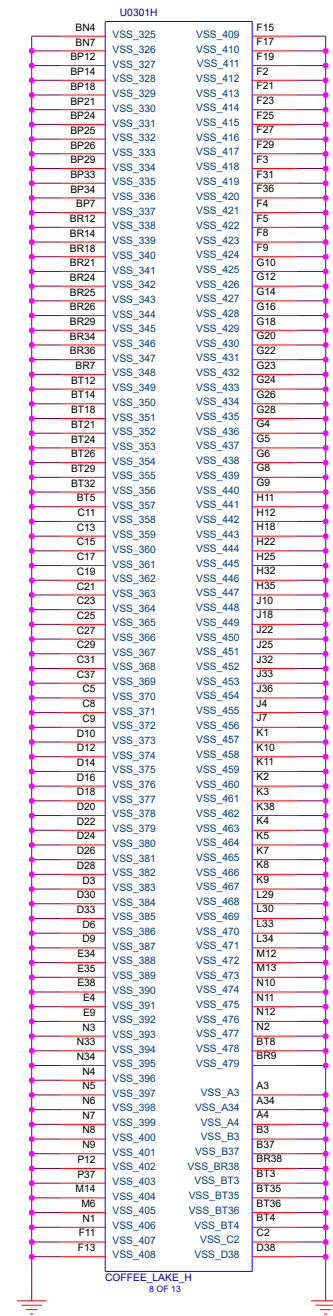
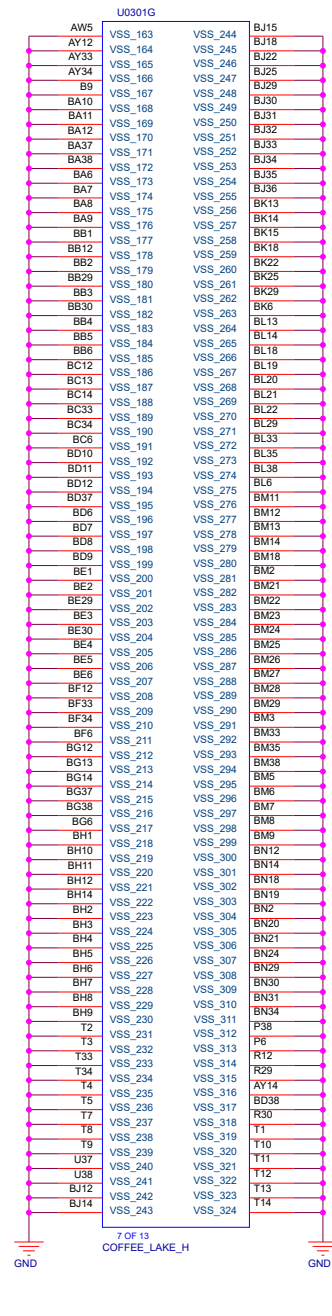
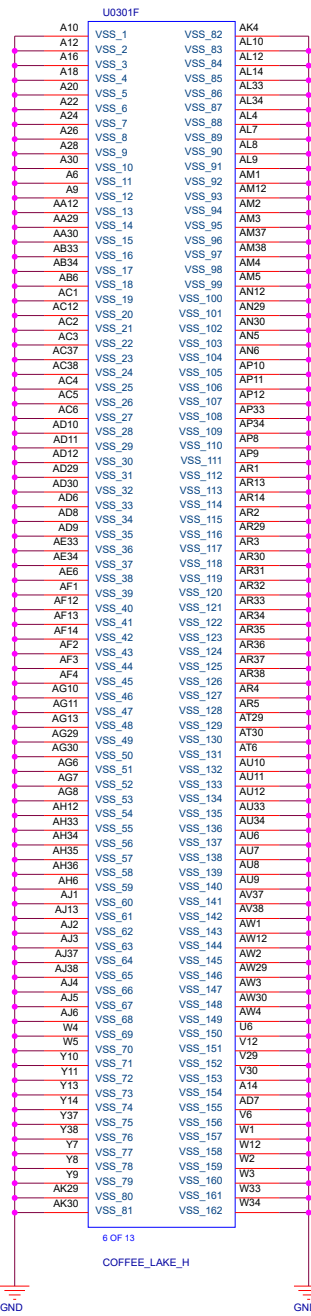
USB3.0 Type C : Right

USB3.0 Type C : Right

USB3.0 Port3 : NIA

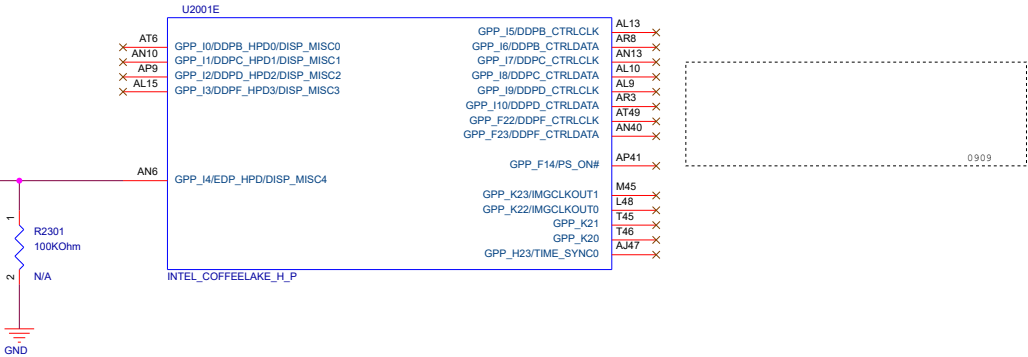
USB3.0 Port4 (Charger)



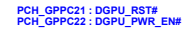
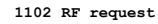


HPD0 to DP
HPD1 to HDMI
HPD2 to TBT
HPD3 to VGA
HPD4 to EDP Panel

Chris



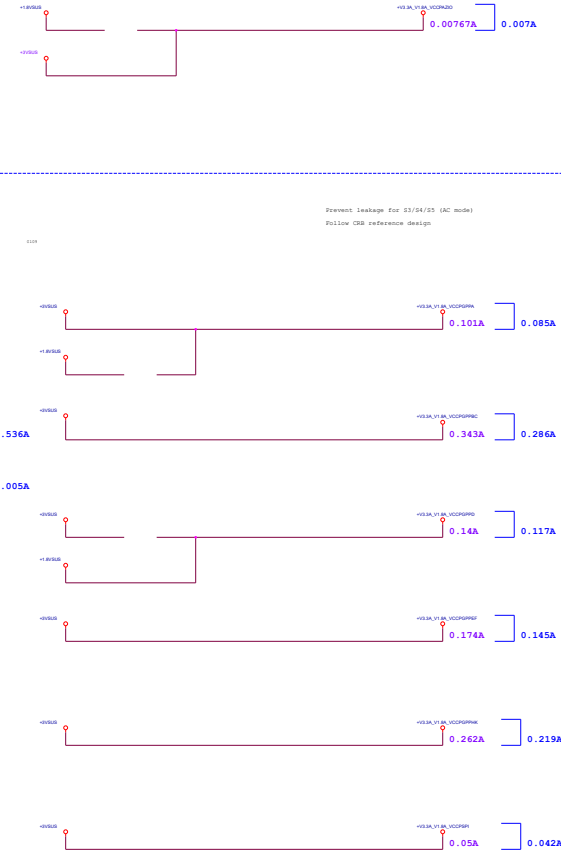
DDP Strap Setting Update:
0 = Port is not detected (Default)
1 = Port is detected



- XTAL_Freq_Select = GPP_I4
- Pin Strap for XTAL frequency selection
- An external 4.7k to 10k Ohm +/-5% pull-up to VCC (1.8V or 3.3V) is required on this strap for PCH 24 MHz XTAL operation

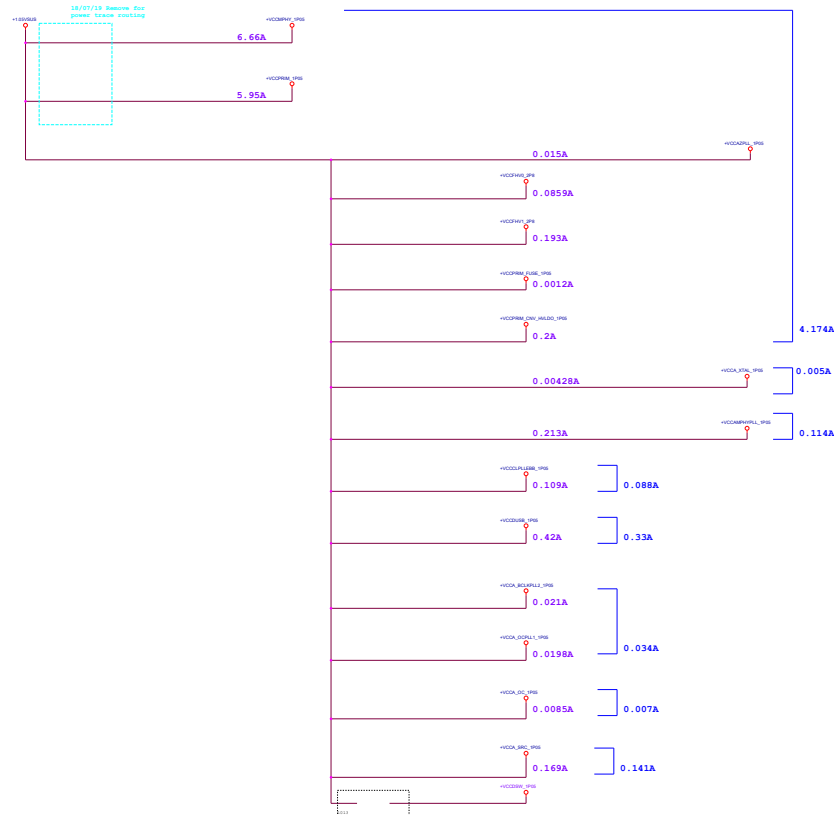
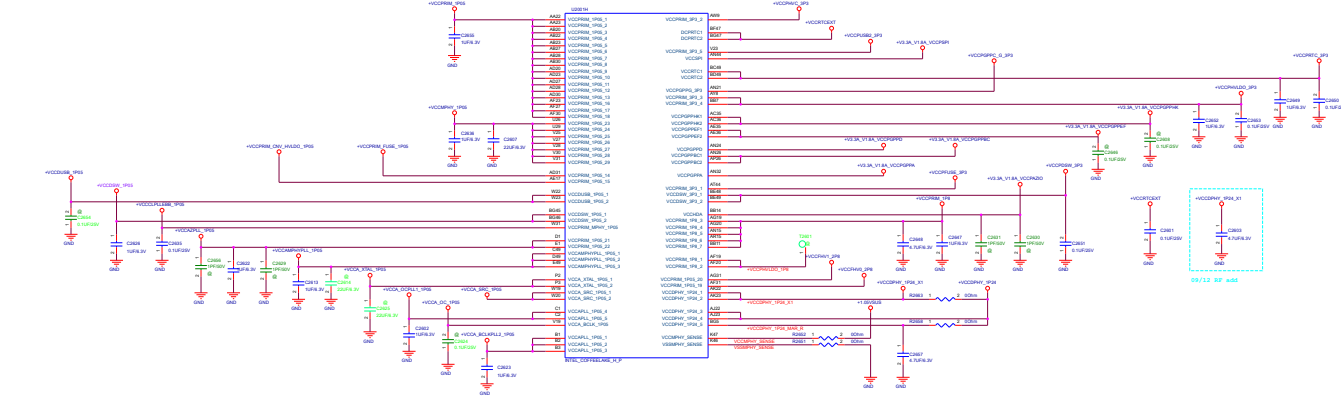
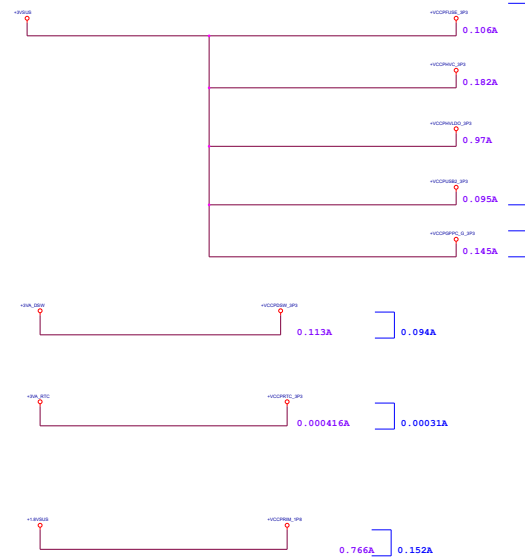
Table 8-1. Power Descriptions for PCH in CNL-H

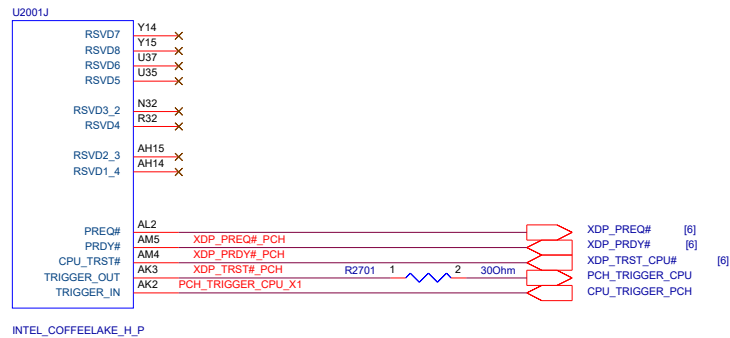
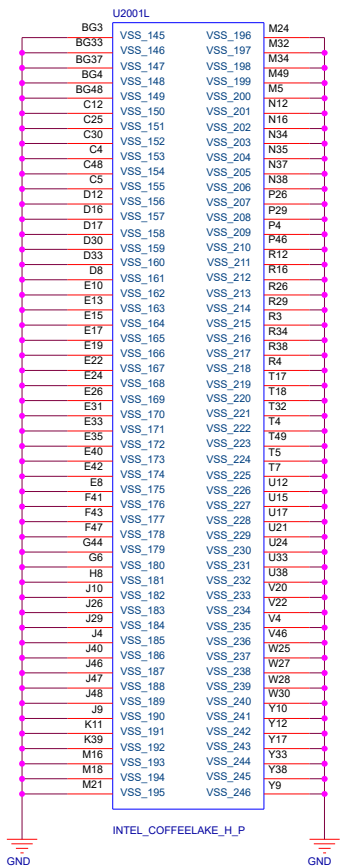
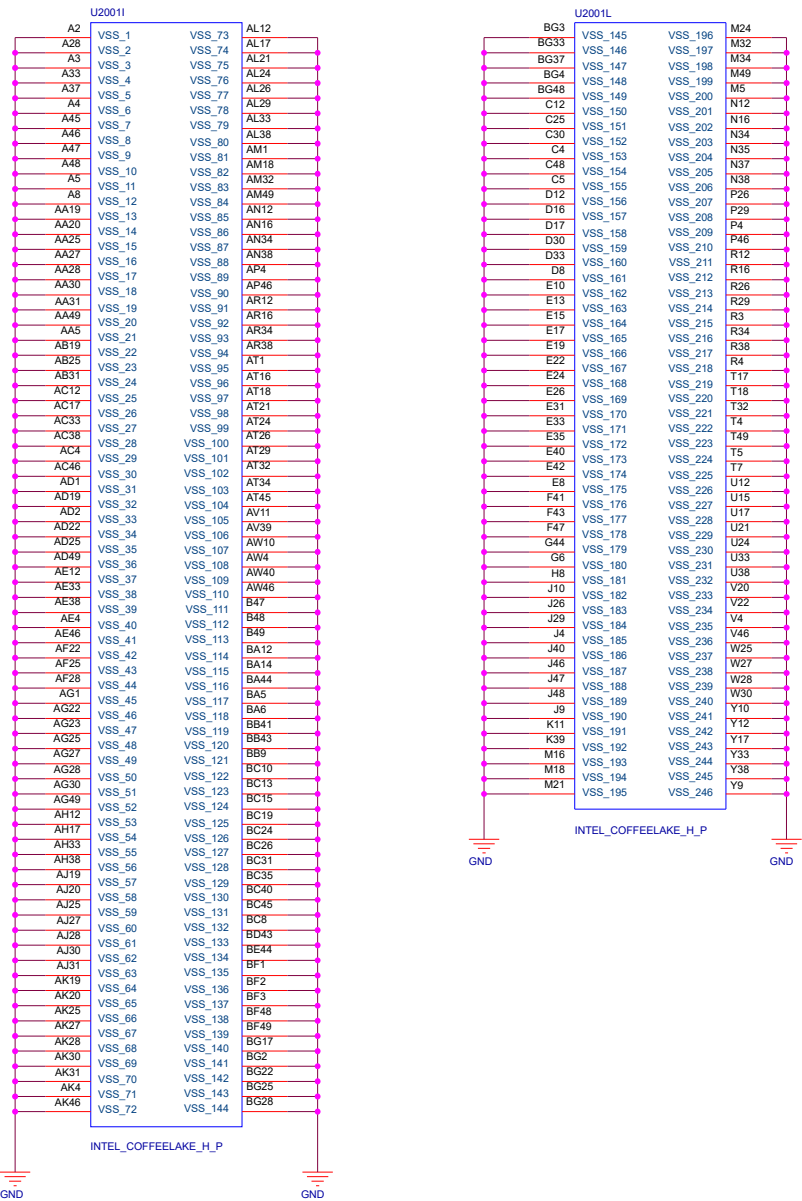
Name	Description
VCCPWHVLD0_1P8	1.8V Primary Well. On the motherboard, this power pin must be connected to VCCPWHVLD0_1P8 rail in Internal 1.8 V VRM Mode and left as no-connect in External 1.8V VRM Mode.
VCCPGPPA	1.8V or 3.3V for GPP_A group.
VCCPGPPBC	1.8V or 3.3V for GPP_B and GPP_C groups.
VCCPGPPD	1.8V or 3.3V for GPP_D group.
VCCPGPPEF	1.8V or 3.3V for GPP_E and GPP_F groups.
VCCPGPPG_3P3	3.3V for GPP_G group.
VCCPGPPHK	1.8V or 3.3V for GPP_H and GPP_K groups.
VCCMPHY_SENSE	1.05V Sense Line.
VSSMPHY_SENSE	0V (Ground) Sense Line.
VSS	Ground.



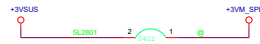
Prevent leakage for S1/S4/S5 (AC mode)
Follow CSB reference design

Purple reference CSB
Blue reference EDS



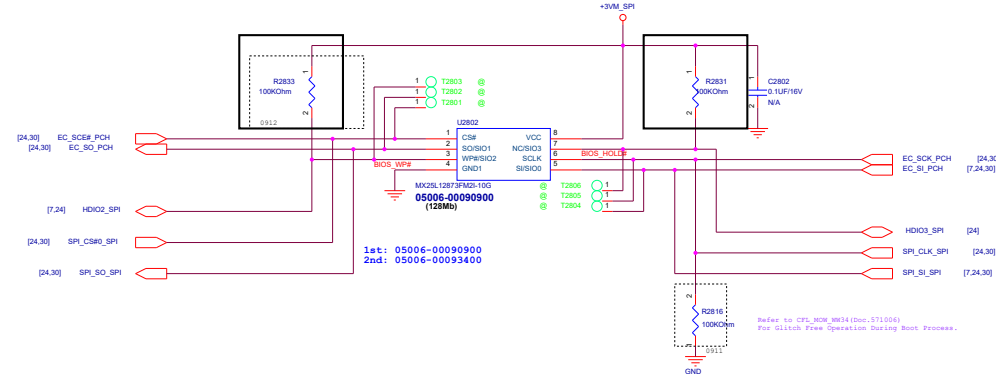


SPI Power



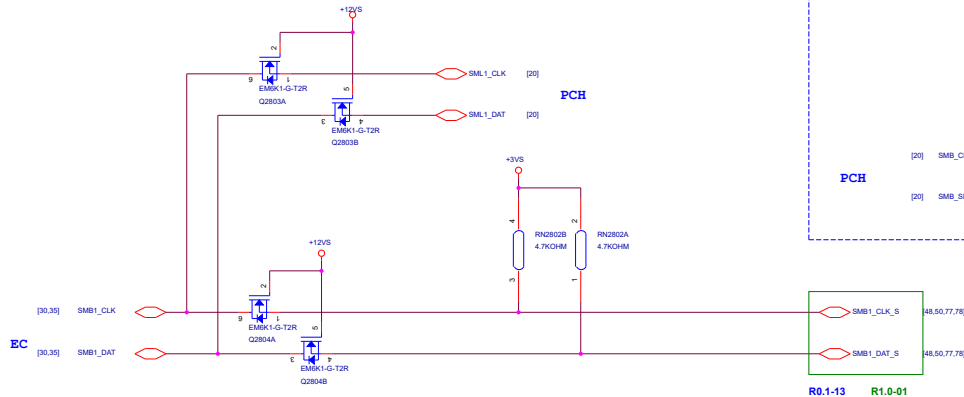
1st SPI ROM

1st: 05006-00090900 FLASH MXIC MX25L12873PM2I-10G 128M SOP-8L
2nd: 05006-00093100 FLASH GD25B127DSIGG IGADEVICE 128MB SOP8

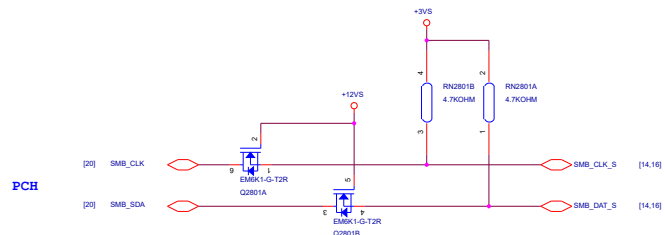


Refer to CPL_ROM_M534(Dec-571006)
For Glitch Free Operation During Boot Process..

System Management Interface

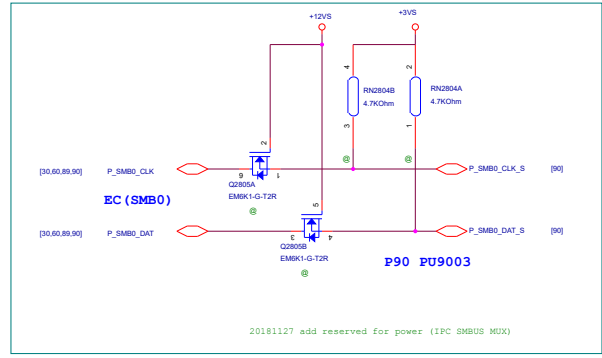


SMBus Interface

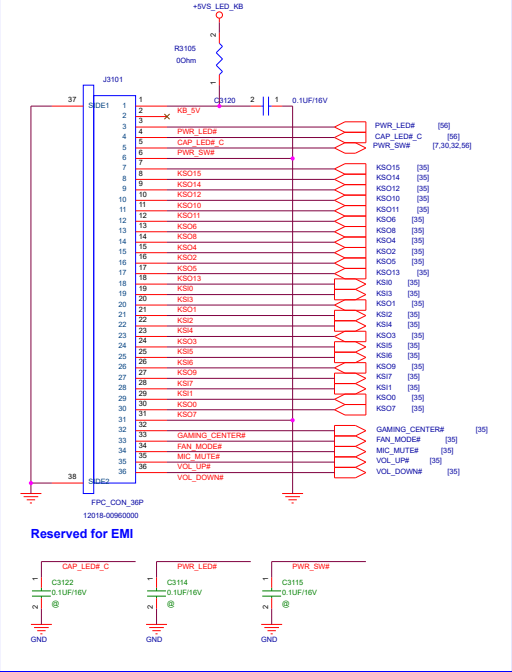


R0.1-13 R1.0-01

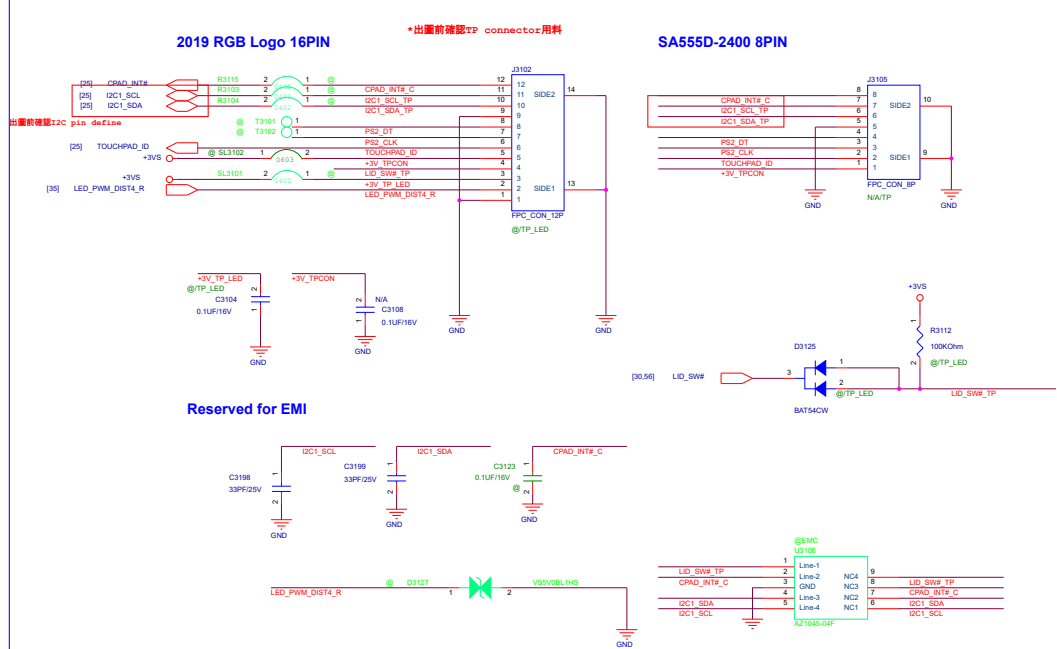
CPU,VGA Thermal Sensor
Power Thermal Sensor



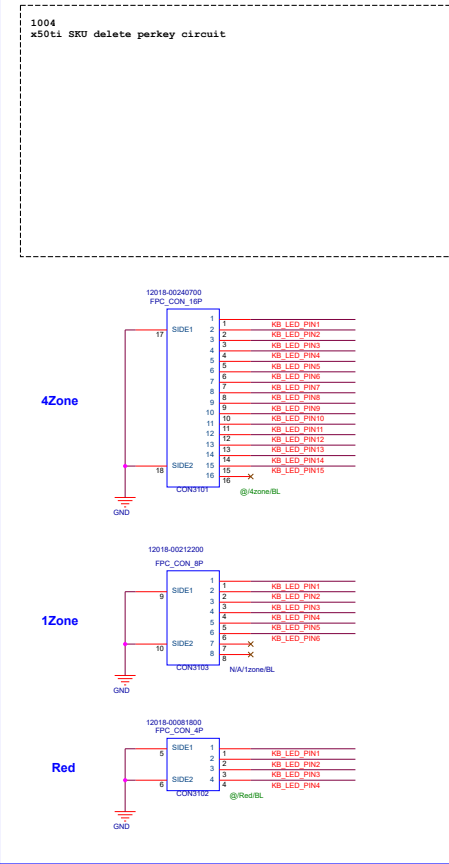
Keyboard Connector



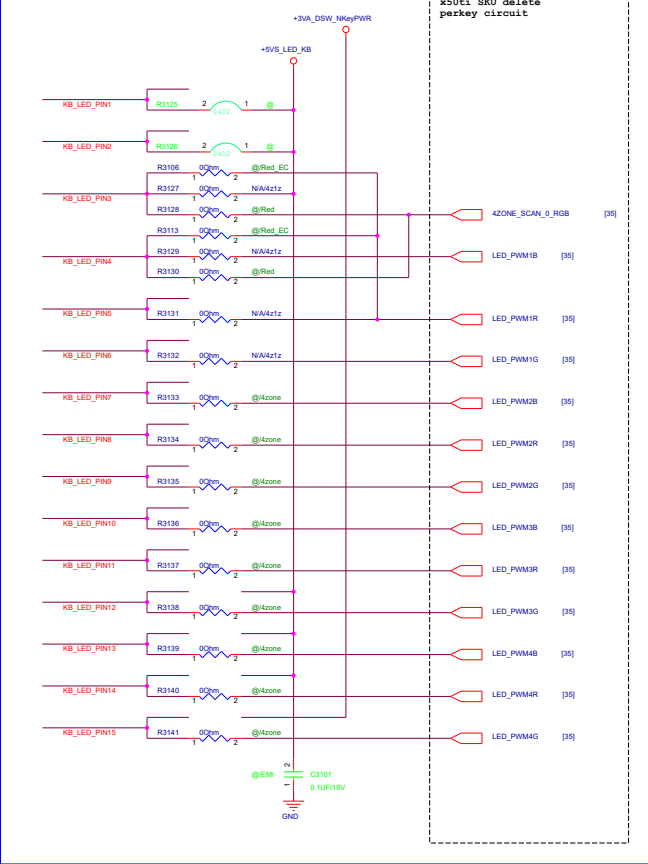
Touch Pad Connector



Keyboard Backlight



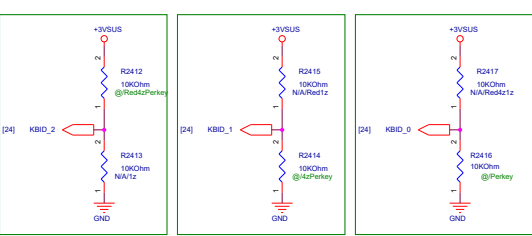
RED, 4zone,1zone, PerKey Co-layout



For EMI



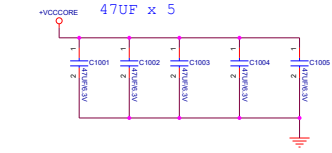
Keyboard ID



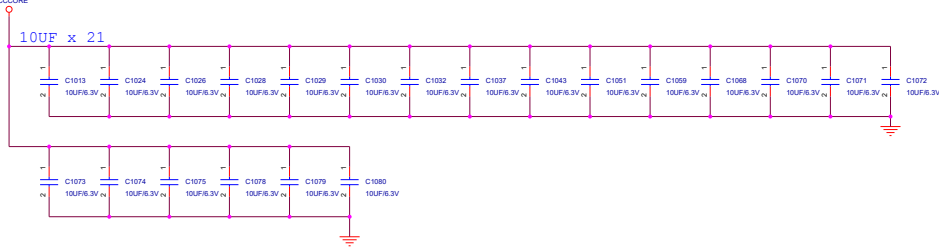
KB ID PCH Side(HW請依照此表格做設計判斷) *BIOS會再反向				
Code	ROG RGB KB Type	KBID 2	KBID 1	KBID 0
		(GPP_H18)	(GPP_H17)	(GPP_H16)
0x00	Normal Keyboard	H	H	H
0x01	QWERTASD Partition Keyboard	H	H	L
0x02	4 Zone RGB Keyboard	H	L	H
0x03	Per Key RGB Keyboard	H	L	L
0x04	1 Zone RGB Keyboard	L	H	H

	RED-4pin	1zone RGB_8pin	4zone-16pin	per key-20pin
pin1	VCC	VCC green	VCC green	COM7
pin2	VCC	VCC red	VCC red	COM6
pin3	GND	VCC blue	VCC blue	COM5
pin4	GND	LED1 blue	LED1 blue	COM4
pin5		LED1 red	LED1 red	COM3
pin6		LED1 green	LED1 green	COM2
pin7		NC	LED2 blue	COM1
pin8		NC	LED2 red	COM0
pin9			LED2 green	GND
pin10			LED3 blue	GND
pin11			LED3 red	GND
pin12			LED3 green	VCC
pin13			LED4 blue	VCC
pin14			LED4 red	VCC
pin15			LED4 green	VDD-33
pin16			NC	NC
pin17				GCLK
pin18				SDI
pin19				DCLK
pin20				LE

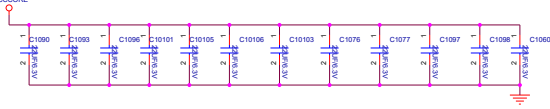
+VCCORE near CPU



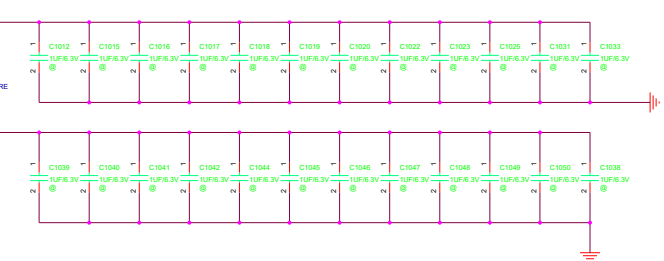
+VCCORE DECAPS Place Back Side (TOP)



22uF x 12



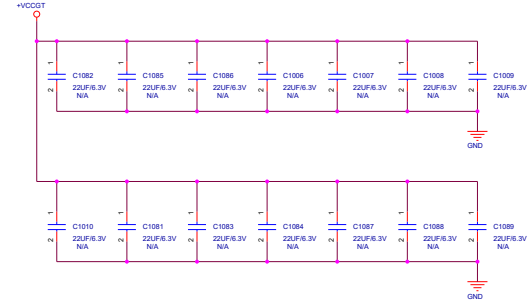
1uF x 24



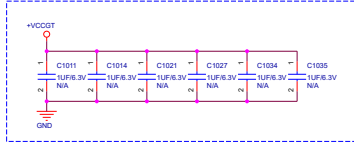
Domain	Board Edge cap	Backside cap	Notes
Vcc	5x 47uF 0805		
		12x 22uF 0603	
		21x 10uF 0402	
		24x 1uF 0201	
		24x 0201 (placeholder)	
VccGT	3x 47uF 0805		Place as close to the BGA as possible
	7x 22uF 0603		
		10x 10uF 0402	
		12x 1uF 0201	

+VCCGT cap near CPU

22uF x14



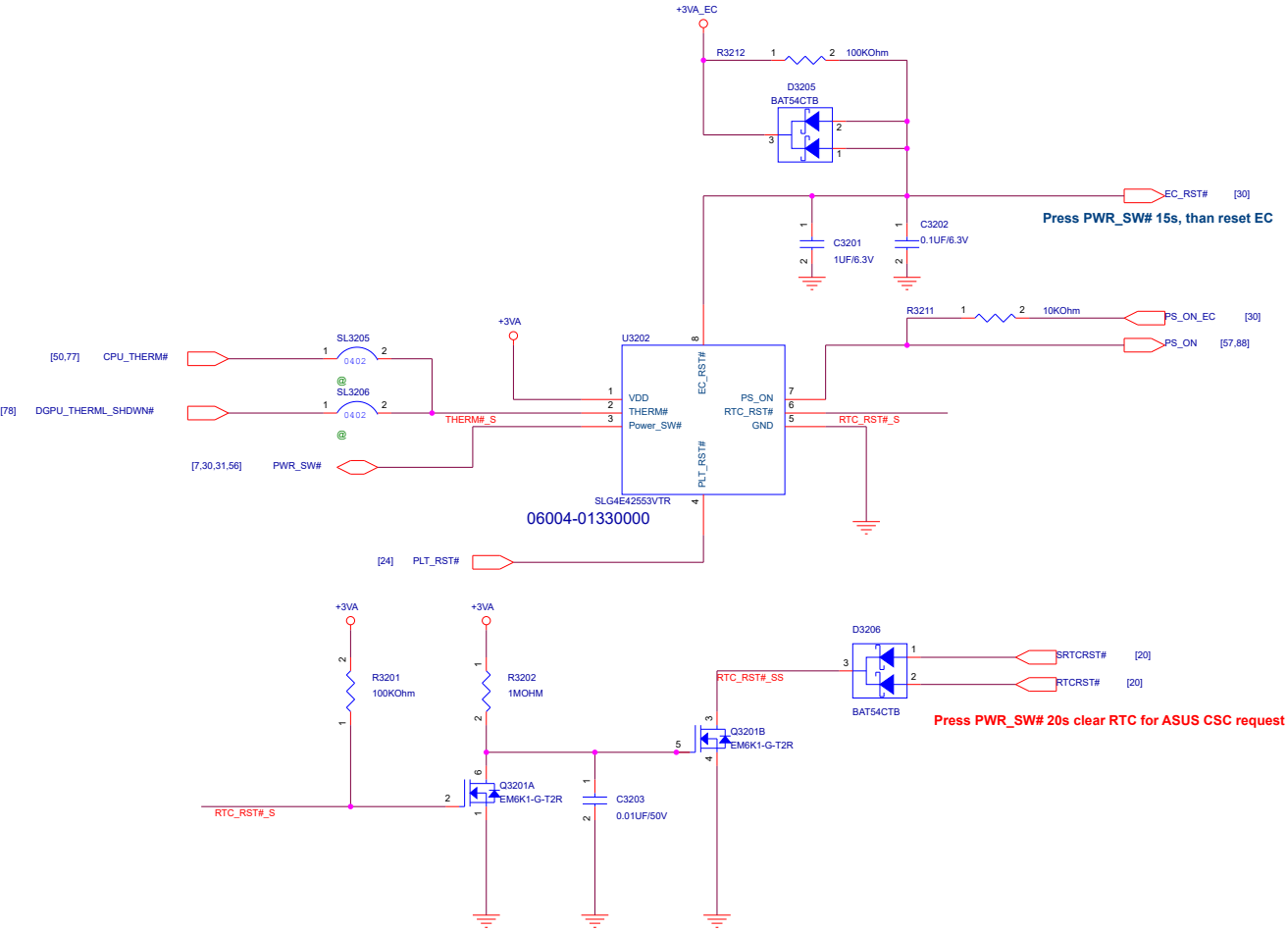
1107 add for VCCGT PI issue



Modern standby project should use Silego solution for EC/RTC reset (Microsoft hardware requirements)

6.6.2 Power button behavior

<https://docs.microsoft.com/en-us/windows-hardware/design/minimum/minimum-hardware-requirements-overview#section-60---shared-minimum-hardware-requirements-for-components>
UX362FA R1.3 board will verify this circuit 7/E



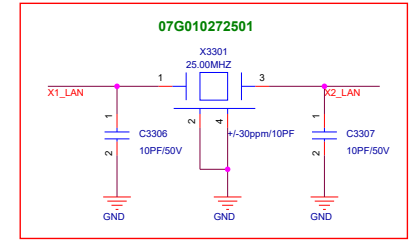
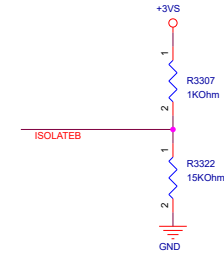
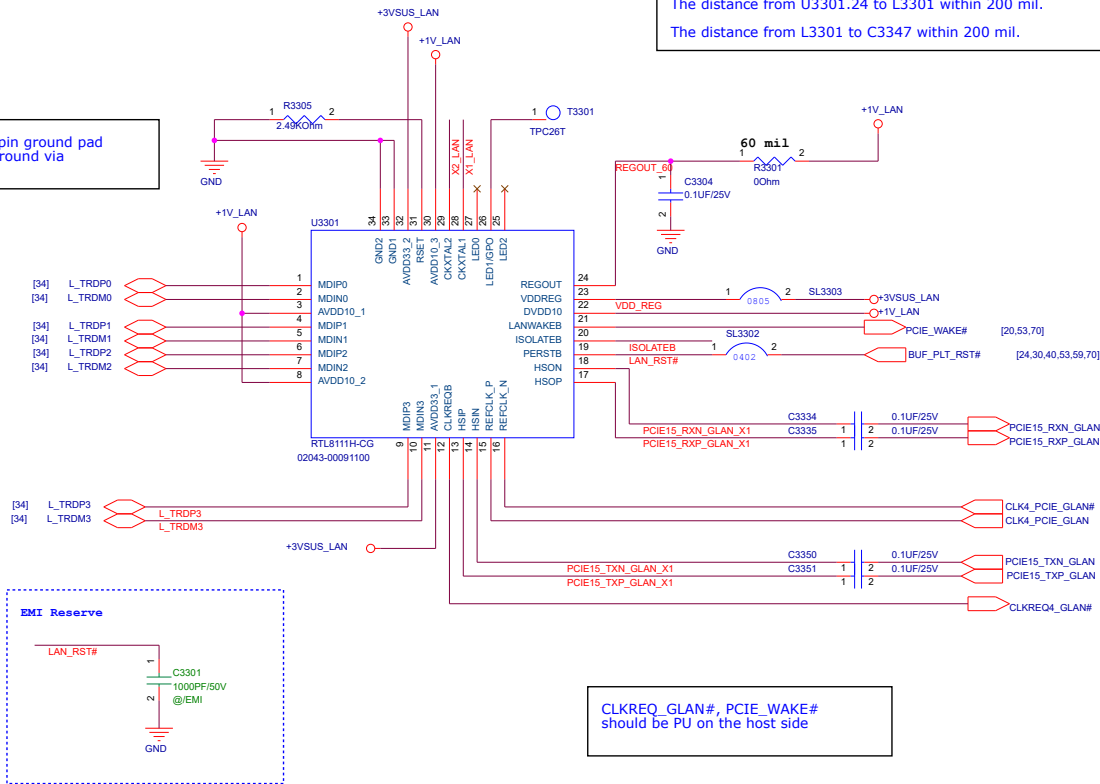
<Variant Name>

		Title : RST_Reset Circuit	
ASUSTeK COMPUTER		Engineer: Gaming RD	

Size	Project Name	G711GW		Rev
B				1.0

The distance from U3301.24 to L3301 within 200 mil.
The distance from L3301 to C3347 within 200 mil.

33/34 pin ground pad
need ground via

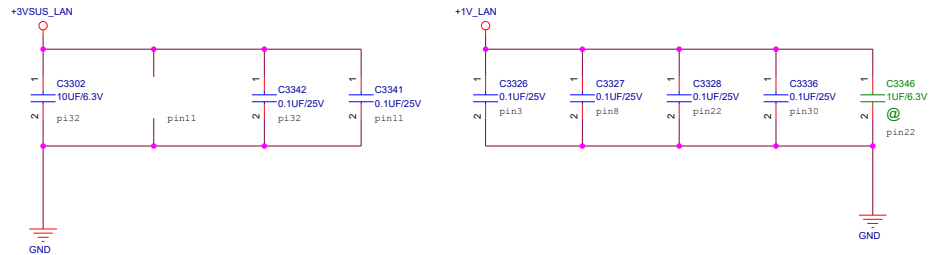
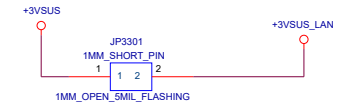


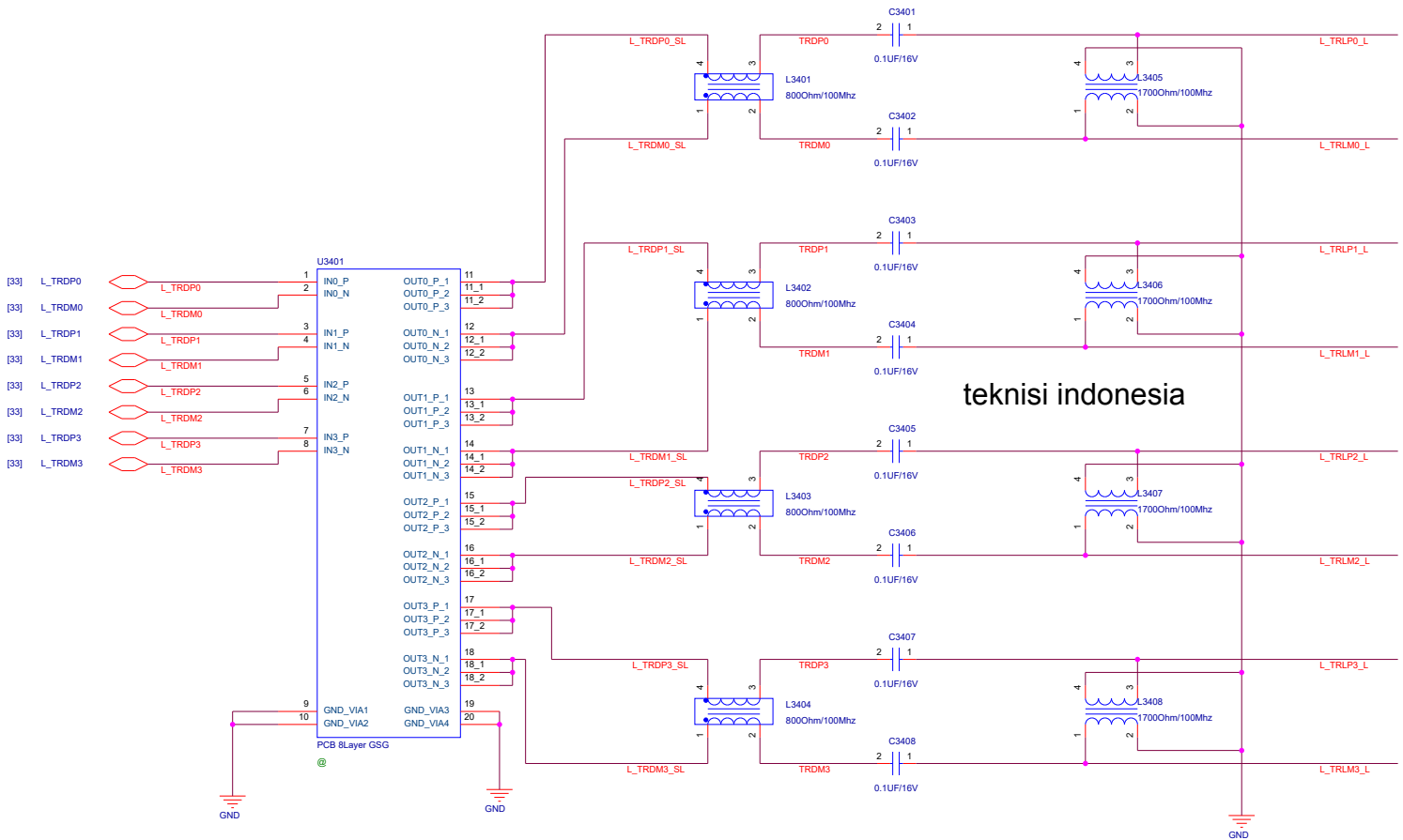
X3301: 25MHZ +/-30ppm/10pF (3225)

1st: P/N:07G010272501 TXC/7V25000011

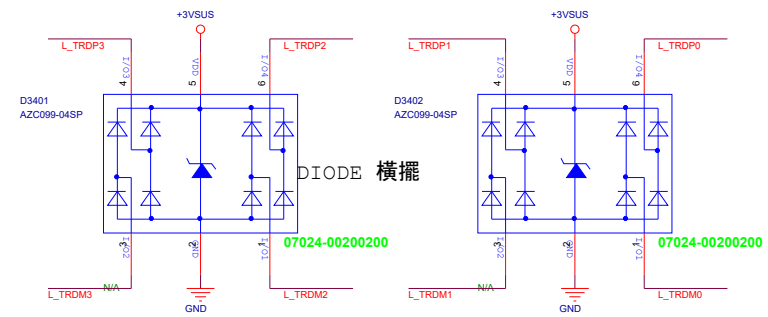
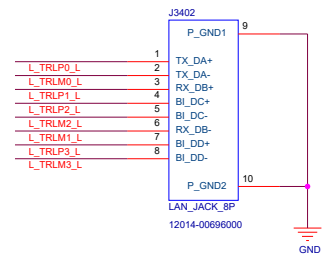
2nd: P/N:07G010952500 HOSONIC/E3FB25

Realtek suggests 3V_LAN raise time >1ms

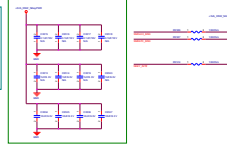
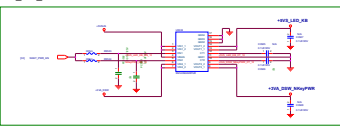




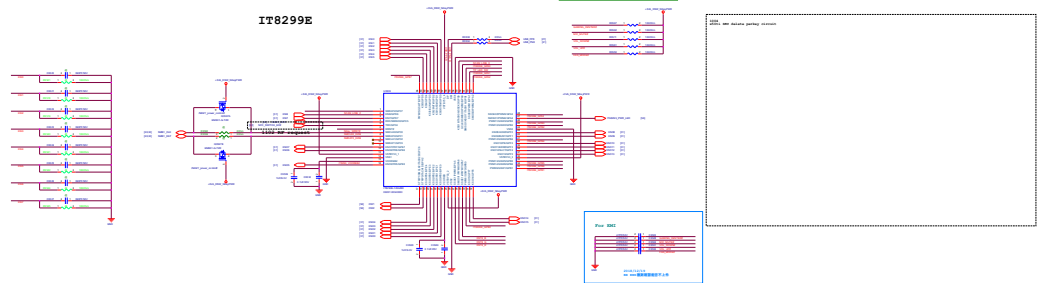
LAN Connector



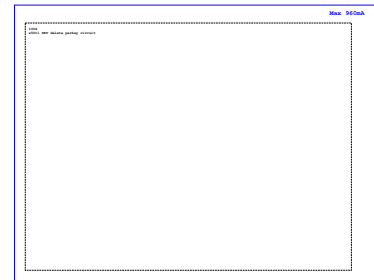
D3401,D3402 ESD Diode
1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP.R7G
2nd Source: P/N:07024-00710000 NXP/PUSB2X4D



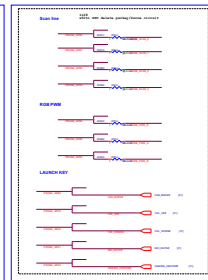
IT8299E



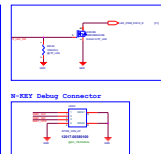
KB RGB Per Key LED



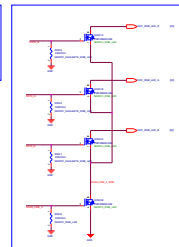
KB RGB co-layout



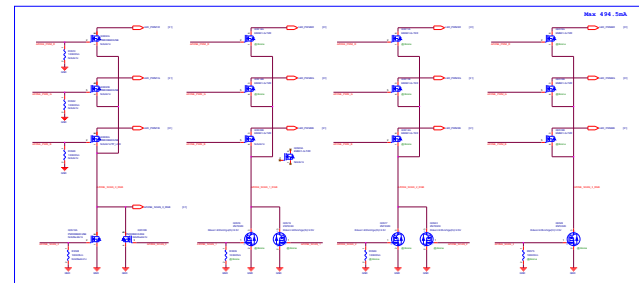
TP LED



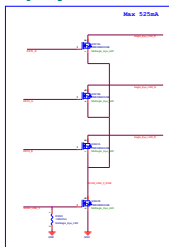
NFC RGB LED



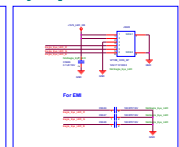
KB RGB 4Zone and 1Zone LED



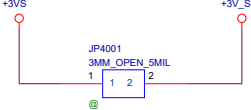
Eagle Eye LED



Eagle Eye LED Conn



NGFF_SSD



PCIE9
NGFF1 PCIE Lane3

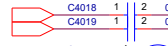
[21] PCIE9_RXN_NGFF1_L0
[21] PCIE9_RXP_NGFF1_L0



PCIE9_RXN_NGFF1_L0_X1
PCIE9_RXP_NGFF1_L0_X1

PCIE10
NGFF1 PCIE Lane2

[21] PCIE9_TXN_NGFF1_L0
[21] PCIE9_TXP_NGFF1_L0



PCIE9_TXN_NGFF1_L0_X1
PCIE9_TXP_NGFF1_L0_X1

PCIE11
NGFF1 PCIE Lane1

[21] PCIE10_RXN_NGFF1_L1
[21] PCIE10_TXP_NGFF1_L1



PCIE10_RXN_NGFF1_L1_X1
PCIE10_TXP_NGFF1_L1_X1

[21] PCIE11_RXN_NGFF1_L2
[21] PCIE11_TXP_NGFF1_L2



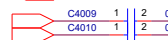
PCIE11_RXN_NGFF1_L2_X1
PCIE11_TXP_NGFF1_L2_X1

[21] PCIE12_RXN_NGFF1_L3
[21] PCIE12_TXP_NGFF1_L3



PCIE12_RXN_NGFF1_L3_X1
PCIE12_TXP_NGFF1_L3_X1

[21] CLK6_PCIE_NGFF1#
[21] CLK6_PCIE_NGFF1

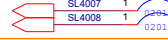


PCIE12_TXN_NGFF1_L3_X1
PCIE12_TXP_NGFF1_L3_X1

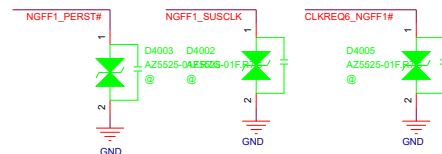
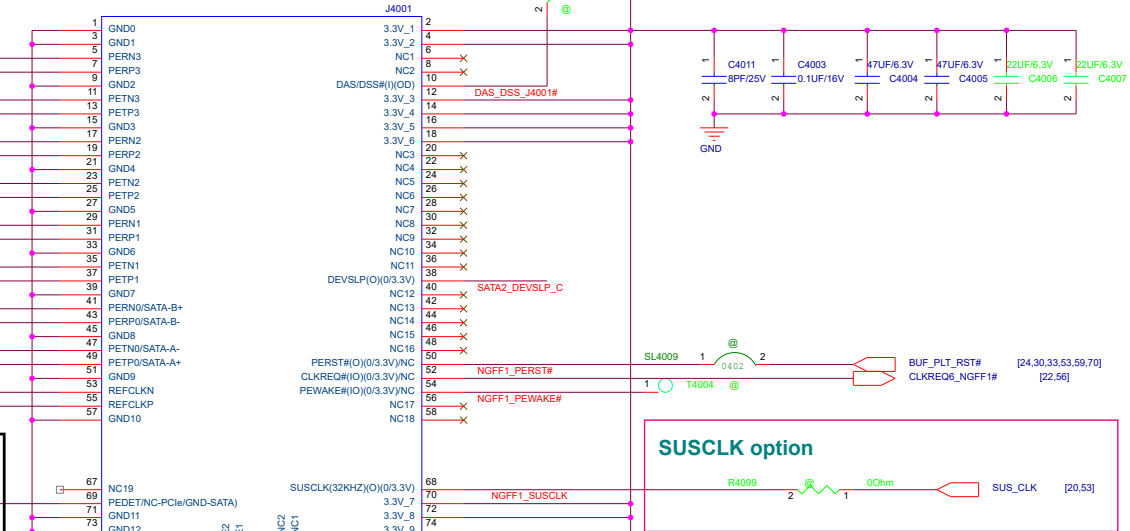
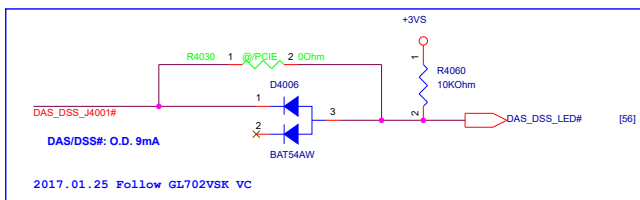
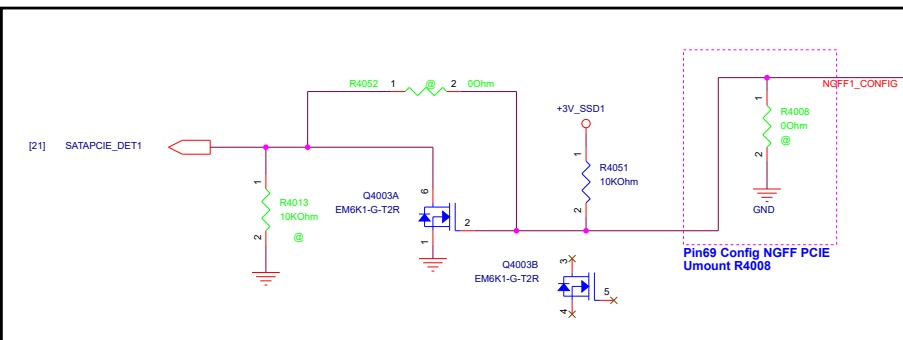
For SATA PCIE colaty, PCIE PN swap

PCIE12/SATA1a
NGFF1 PCIE Lane0
/SATA Port1

[21] PCIE12_RXN_NGFF1_L3
[21] PCIE12_TXP_NGFF1_L3



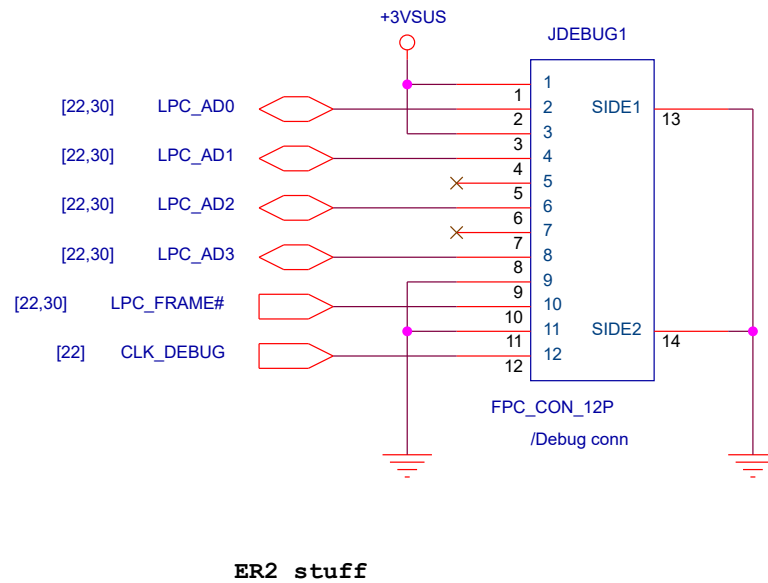
PCIE12_TXN_NGFF1_L3_X1
PCIE12_TXP_NGFF1_L3_X1



<Variant Name>

Project Name		Rev
ASUS G711GW		R1.0
Title : MiniCard_SSD		
Size	Dept.: ASUSTek COMPUTER	Engineer: Gaming RD
B	Date: Tuesday, March 19, 2019	Sheet 40 of 103

LPC Debug Port



<Variant Name>



Title : DEBUG_LPC

ASUSTeK COMPUTER

Engineer: Gaming RD

Size

Project Name

A

G711GW

Rev

1.0

Date: Tuesday, March 19, 2019

Sheet 44 of 103

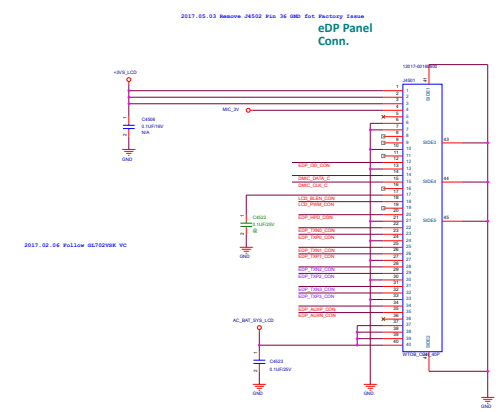
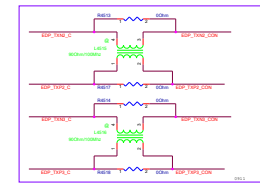
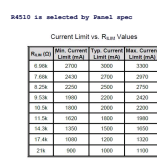
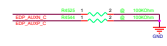
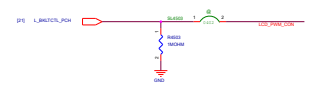
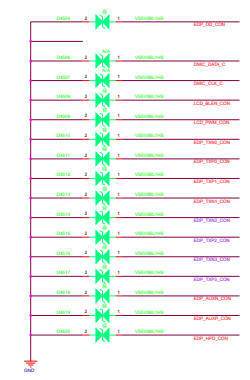
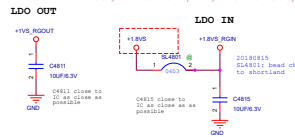


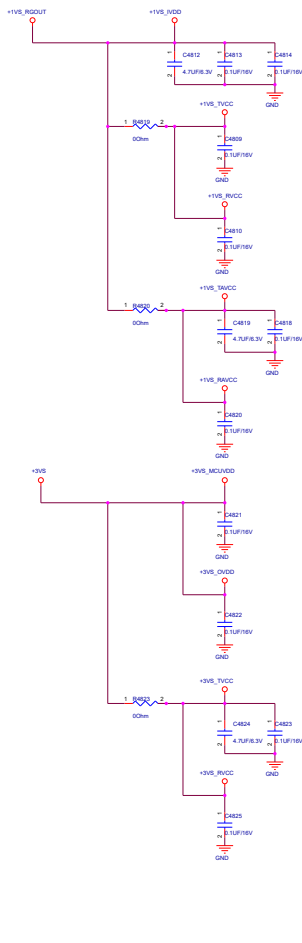
Figure 1: Schematic representation of the genomic organization of the genes. The figure shows the structure of several genes and their transcripts. Genes are represented by red boxes, and transcripts by blue lines. The genes are: EGP_TNPO, EGP_TNPO2, EGP_TNPO3, EGP_TNPO4, EGP_TNPO5, EGP_TNPO6, EGP_TNPO7, EGP_TNPO8, EGP_TNPO9, EGP_TNPO10, EGP_TNPO11, EGP_TNPO12, EGP_TNPO13, EGP_TNPO14, EGP_TNPO15, EGP_TNPO16, EGP_TNPO17, EGP_TNPO18, EGP_TNPO19, EGP_TNPO20, EGP_TNPO21, EGP_TNPO22, EGP_TNPO23, EGP_TNPO24, EGP_TNPO25, EGP_TNPO26, EGP_TNPO27, EGP_TNPO28, EGP_TNPO29, EGP_TNPO30, EGP_TNPO31, EGP_TNPO32, EGP_TNPO33, EGP_TNPO34, EGP_TNPO35, EGP_TNPO36, EGP_TNPO37, EGP_TNPO38, EGP_TNPO39, EGP_TNPO40, EGP_TNPO41, EGP_TNPO42, EGP_TNPO43, EGP_TNPO44, EGP_TNPO45, EGP_TNPO46, EGP_TNPO47, EGP_TNPO48, EGP_TNPO49, EGP_TNPO50, EGP_TNPO51, EGP_TNPO52, EGP_TNPO53, EGP_TNPO54, EGP_TNPO55, EGP_TNPO56, EGP_TNPO57, EGP_TNPO58, EGP_TNPO59, EGP_TNPO60, EGP_TNPO61, EGP_TNPO62, EGP_TNPO63, EGP_TNPO64, EGP_TNPO65, EGP_TNPO66, EGP_TNPO67, EGP_TNPO68, EGP_TNPO69, EGP_TNPO70, EGP_TNPO71, EGP_TNPO72, EGP_TNPO73, EGP_TNPO74, EGP_TNPO75, EGP_TNPO76, EGP_TNPO77, EGP_TNPO78, EGP_TNPO79, EGP_TNPO80, EGP_TNPO81, EGP_TNPO82, EGP_TNPO83, EGP_TNPO84, EGP_TNPO85, EGP_TNPO86, EGP_TNPO87, EGP_TNPO88, EGP_TNPO89, EGP_TNPO90, EGP_TNPO91, EGP_TNPO92, EGP_TNPO93, EGP_TNPO94, EGP_TNPO95, EGP_TNPO96, EGP_TNPO97, EGP_TNPO98, EGP_TNPO99, EGP_TNPO100. The transcripts are labeled with their corresponding gene names and the exon number. The figure also shows the location of the genes on the chromosome, with the EGP_TNPO gene being the largest and the EGP_TNPO100 gene being the smallest. The figure is a schematic representation of the genomic organization of the genes, showing the structure of the genes and their transcripts.

[illegible][illegible]

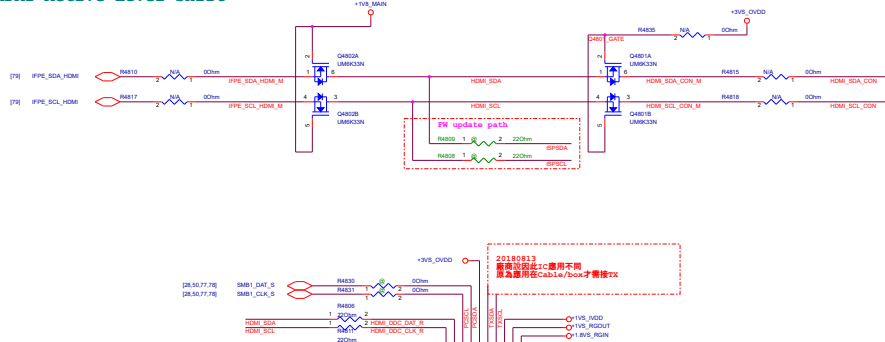
Internal Regulator option



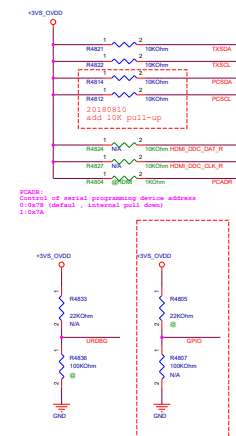
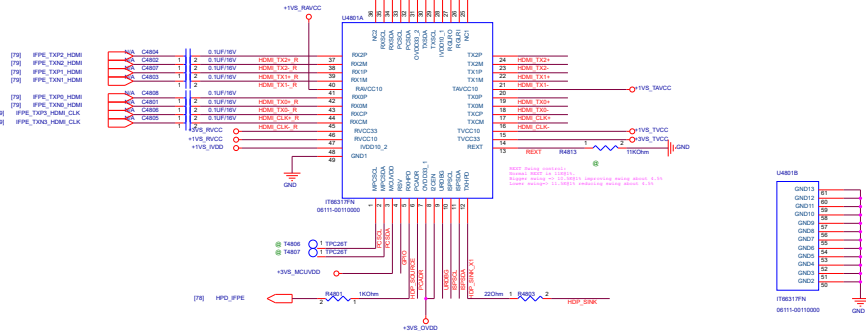
20180815
delete short land



HDMI Active-Level Shift

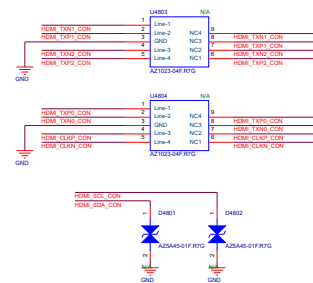


```
20180731
change HDMI retimer to IT66317
```



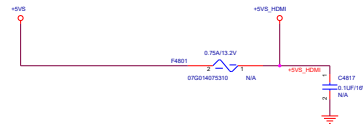
Output Swing	GPIO	URDBG
Level 1 (Lowest)	0	0
Level 2 (Default)	0	1
Level 3	1	0
Level 4 (Highest)	1	1

20180807
add for output swing SW control

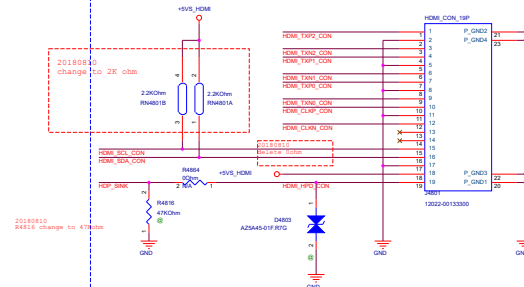


Main Board

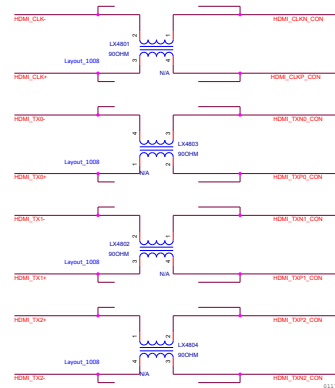
HDMI PWR_+5VS_HDMI



HDMI Conn.



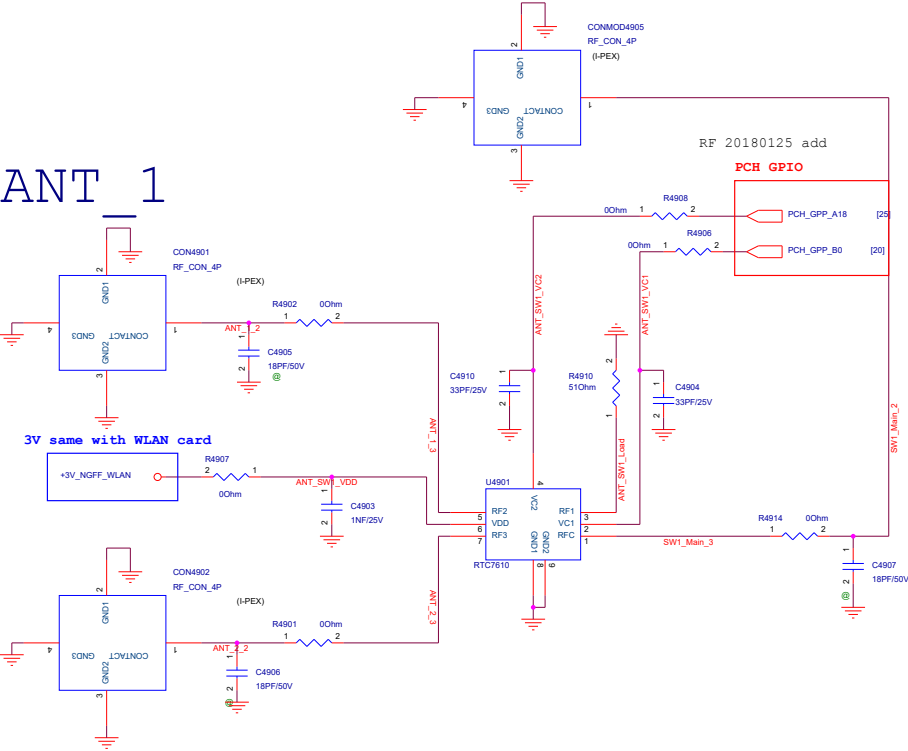
HDMI EMI

20180813
add 90km and choke unmount

N56V C.M Choke : M 09G092090110

Module_AUX

ANT_1

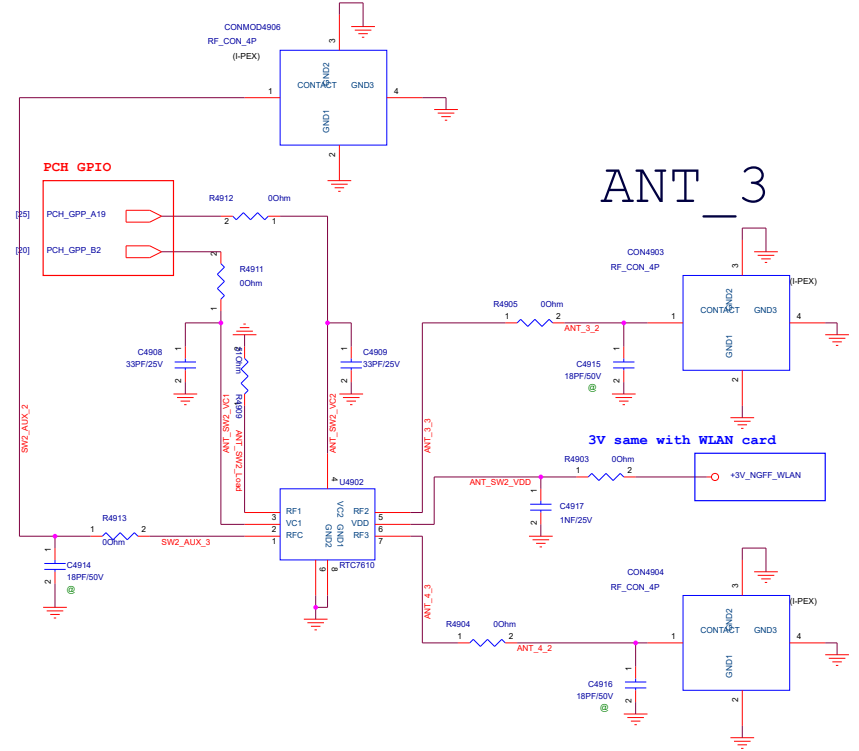


ANT_2

U4901 RTCT610			
ANT	Port	VC1 GPP_B0	VC2 GPP_A18
50 Ω	RF1	1	0
ANT_1	RF2	X	1
ANT_2	RF3	0	0

X: don't care
0: -0.2v~0.3v
1: 1.6v~3.6v

Module_MAIN



ANT_4

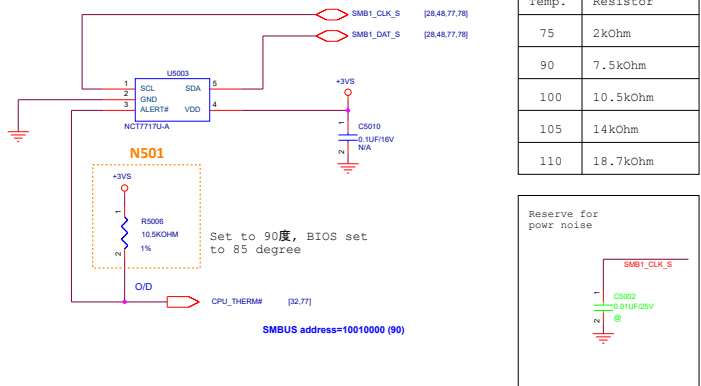
U4902 RTCT610			
ANT	Port	VC1 GPP_B2	VC2 GPP_A19
50 Ω	RF1	1	0
ANT_3	RF2	X	1
ANT_4	RF3	0	0

X: don't care
0: -0.2v~0.3v
1: 1.6v~3.6v

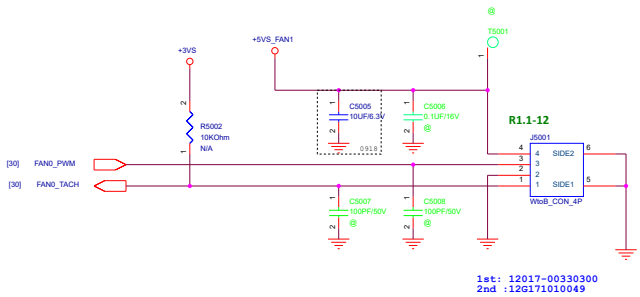
<Core Design>

Project Name		Rev
ASUS GX502GX		1.0
Title : ANT		
Size	Dept.: ASUSTek COMPUTER	Engineer: EE
C	Date: Tuesday, March 19, 2019	Sheet 49 of 103

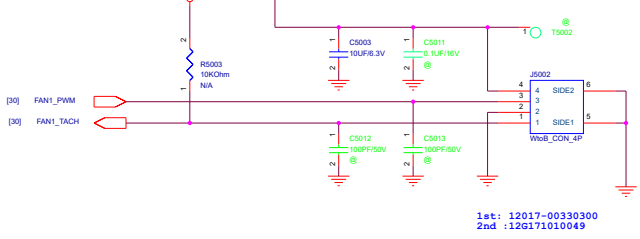
CPU Thermal Sensor

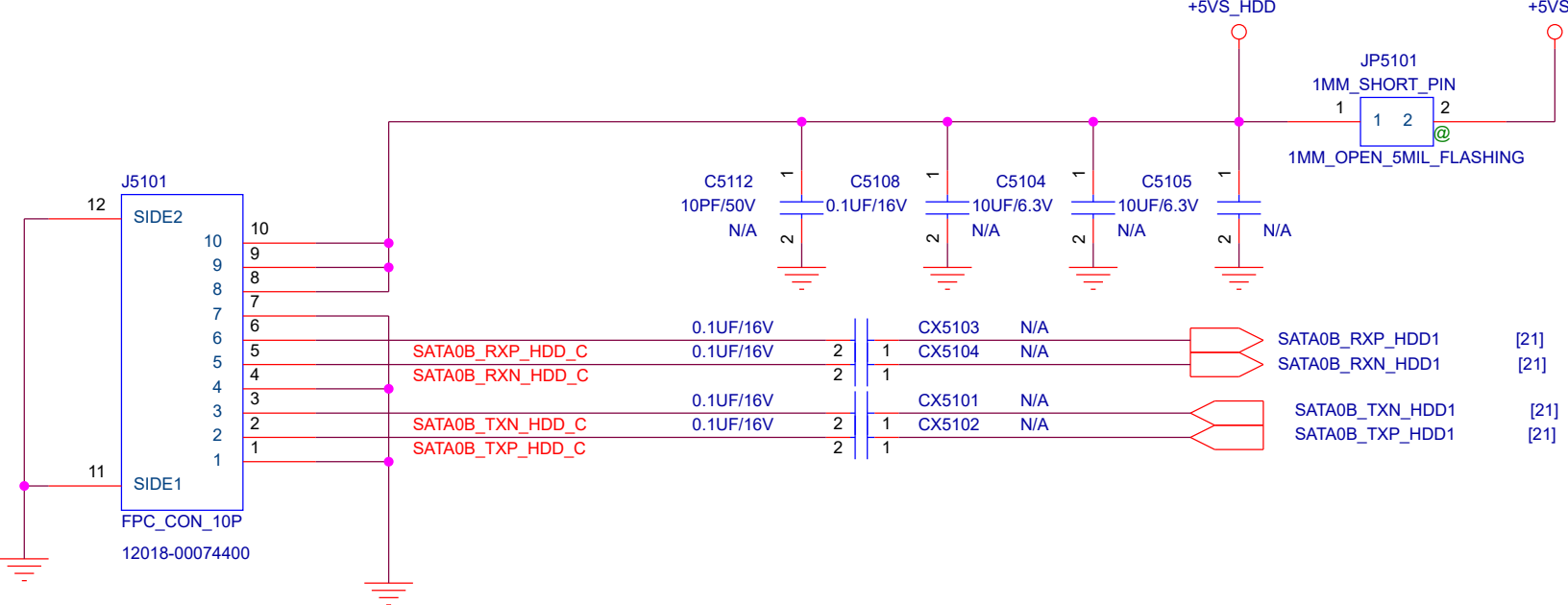


DC FAN Control 1

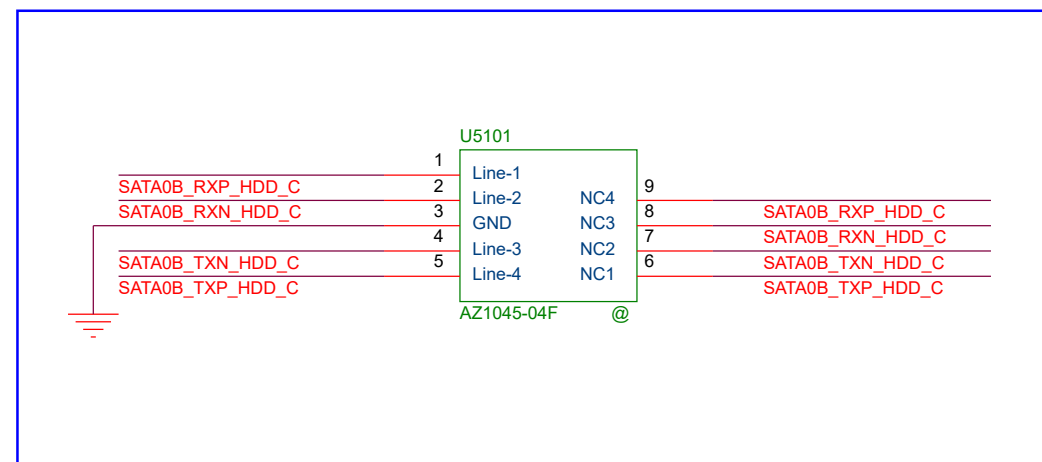


DC FAN Control 2




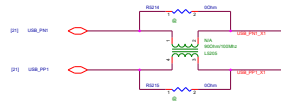
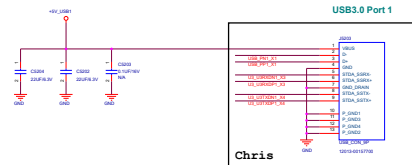


PIN #	Description
1	5V
2	5V
3	5V
4	GND
5	RX+
6	RX-
7	GND
8	TX-
9	TX+
10	GND



<Variant Name>

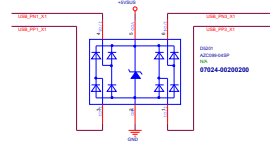
		Title : XDD_HDD & ODD CON	
ASUSTeK COMPUTER		Engineer: Gaming RD	
Size A	Project Name G711GW		Rev R1.0
Date: Tuesday, March 19, 2019	Sheet 51 of 103		



USB3.0 ESD-Protection



USB2.0 ESD-Protection



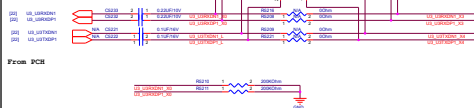
DS98E1 ESD Diode

1st Source: PIN:07G04-0020230 AMAZINGAZC999-04SP.R7G
2nd Source: PIN:07G04-0070000 NXP/USB2X4D

Chris

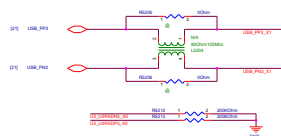
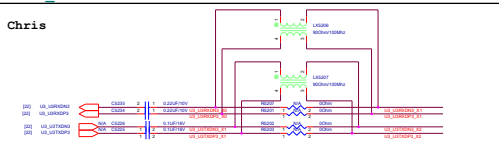
USB3.0 EMI-Protection

13131070
13131071, 13131072, 13131073, 13131074
0902820300400



USB3.0 PORT3

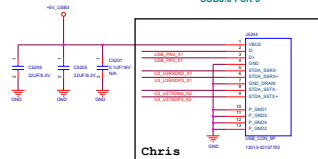
Chris



USB3.0 ESD-Protection



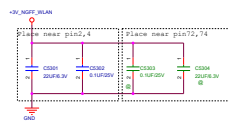
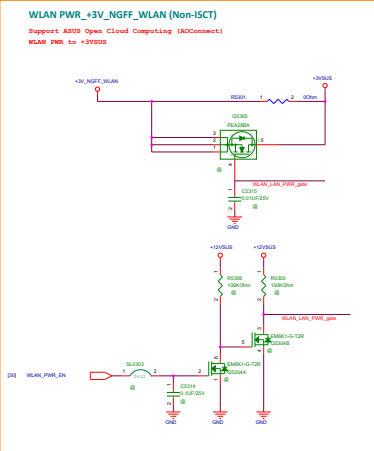
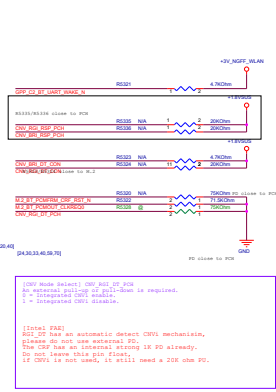
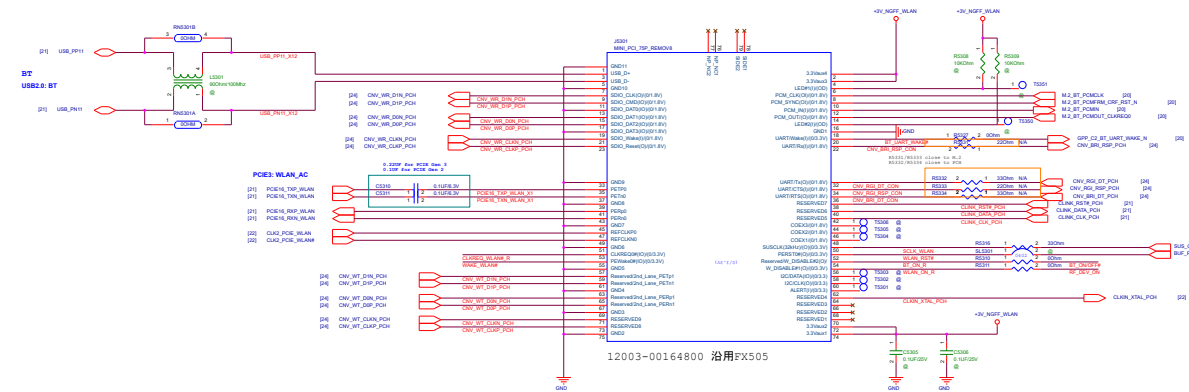
USB3.0 Port 3



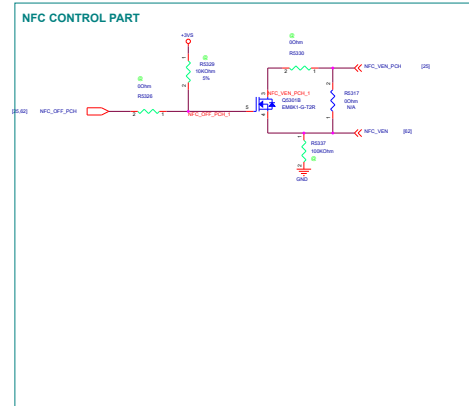
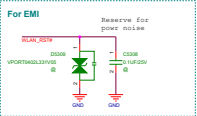
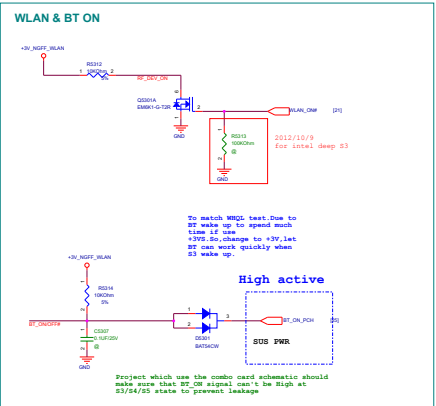
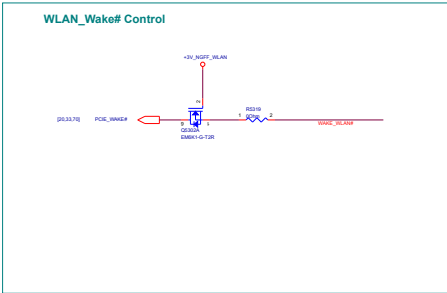
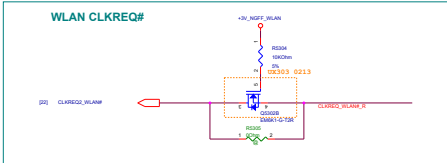
Chris

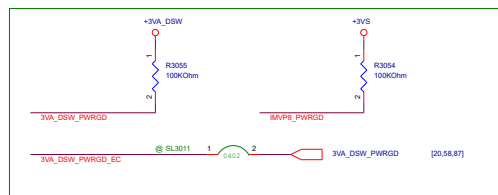
Chris

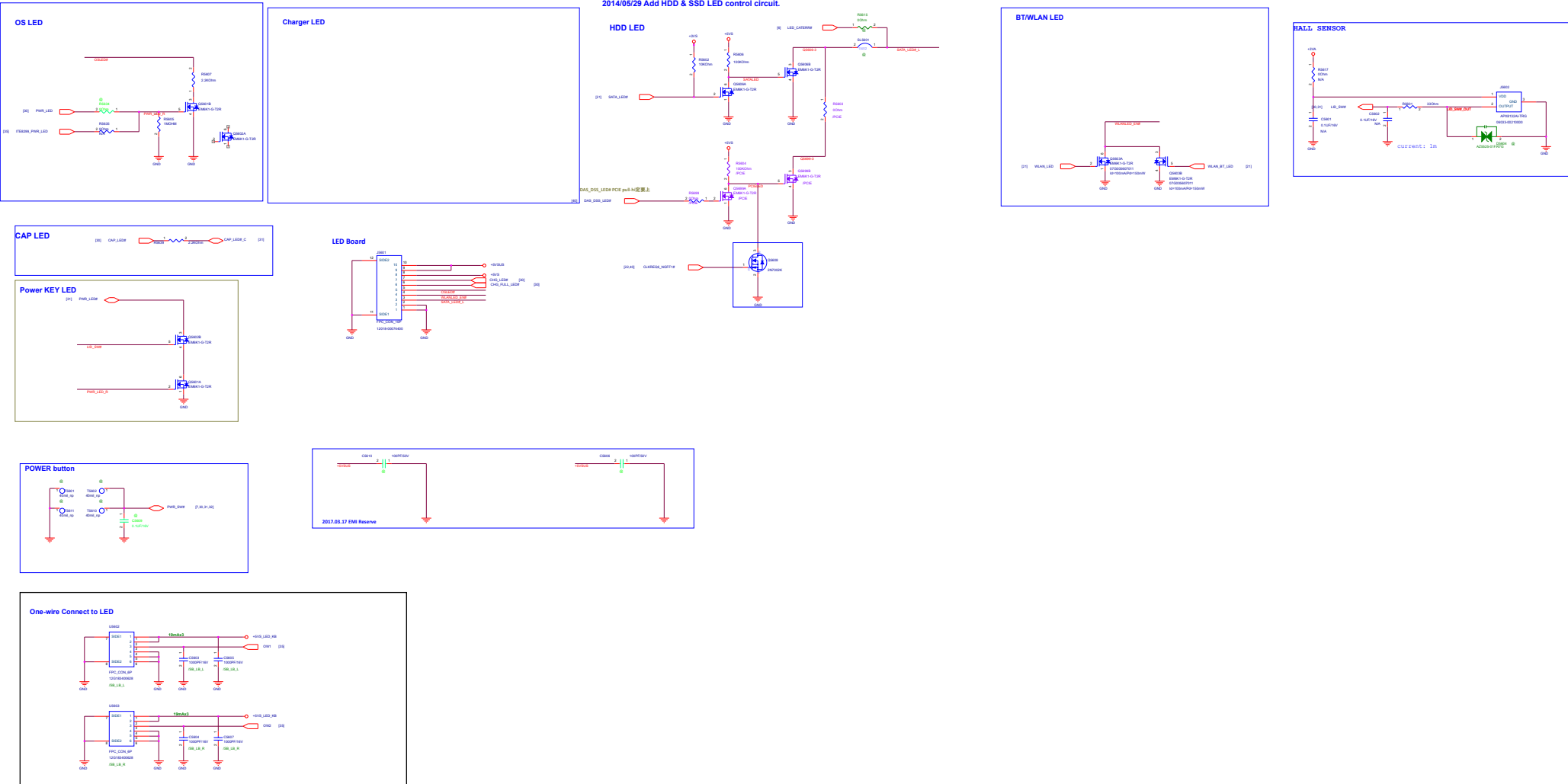
NGFF M.2 TYPE_E-KEY WIFI



J301_NGFF E-KEY WLAN Connector H=2.5mm
1st Source: P/N:1203-0007800 ARGOCTHARS-B0701-TP95
2nd Source: P/N:1203-0007800 DRAGONDATE/C13EBA2ZF8
3rd Source: P/N:1203-0007800 LOTESAPC0062-P001A

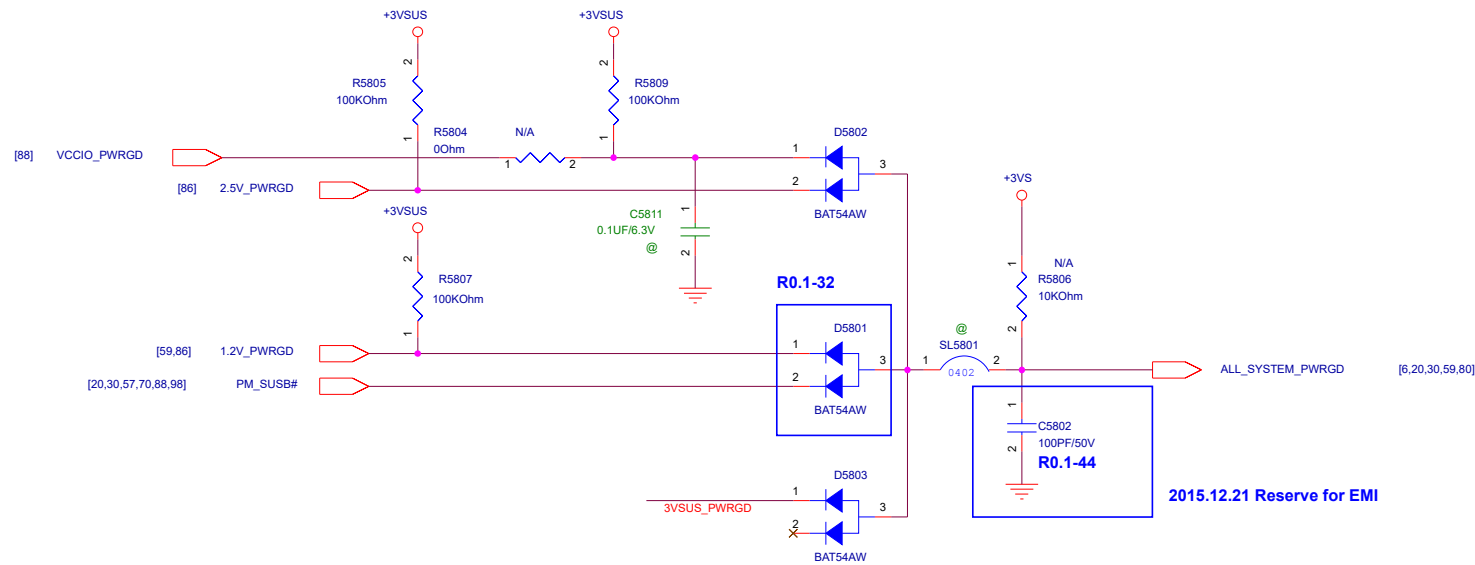
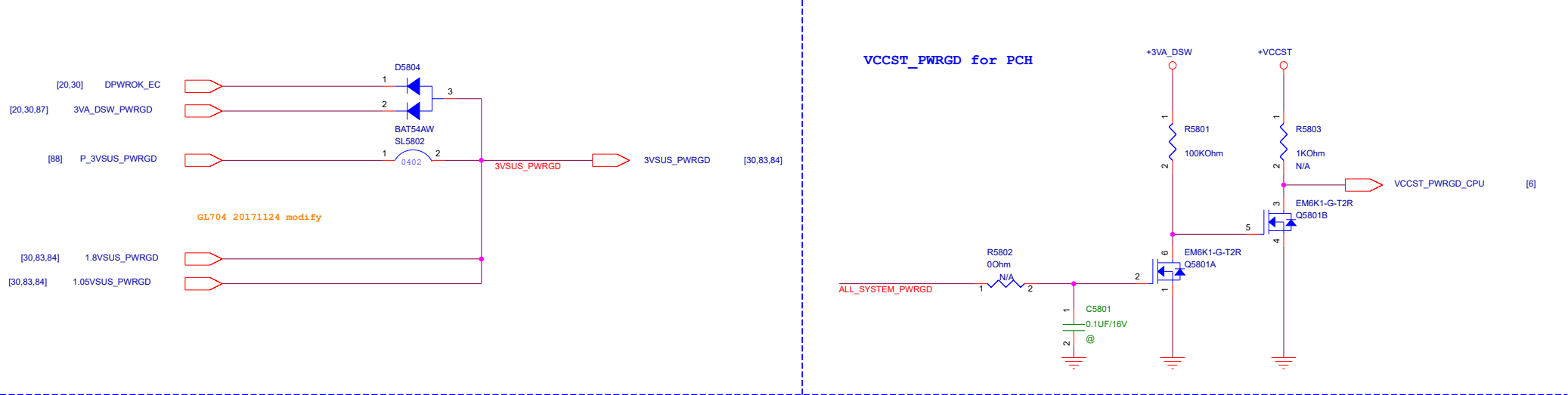







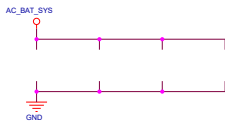
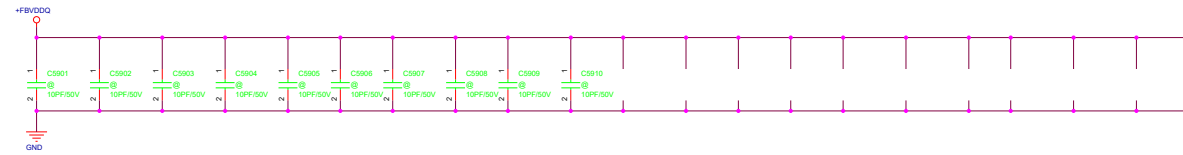
Chris



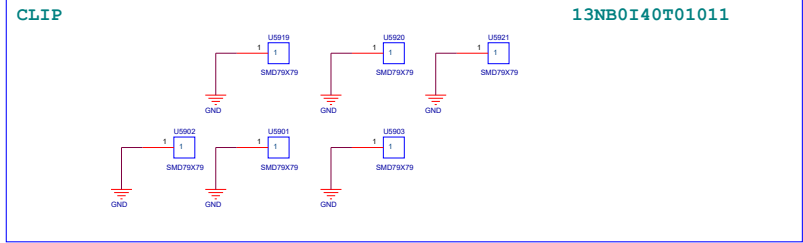
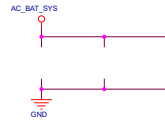


<Variant Name>

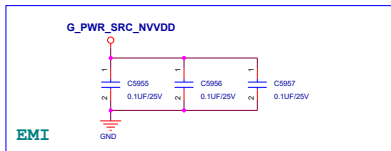
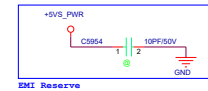
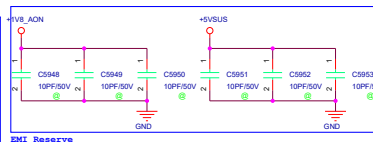
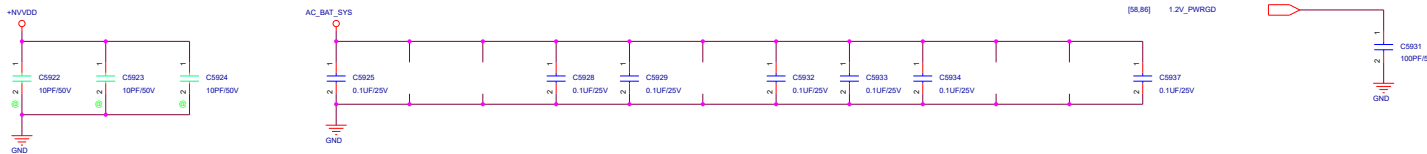
		Title : Power Protect	
ASUSTeK COMPUTER		Engineer: Gaming RD	
Size Custom	Project Name G711GW		Rev 1.0
Date: Tuesday, March 19, 2019		Sheet 58 of 103	



EMI



EMI



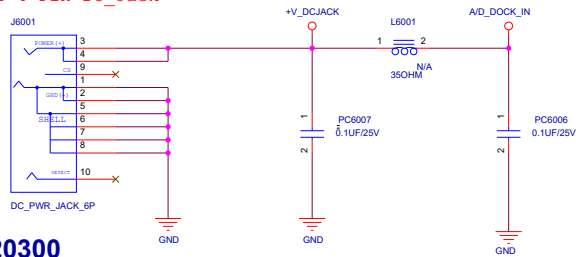
EMI

<Variant Name>

DC-IN Connector

DC Jack使用請詢用River_Hsu

New 6 Phi 4 Pin DC_Jack



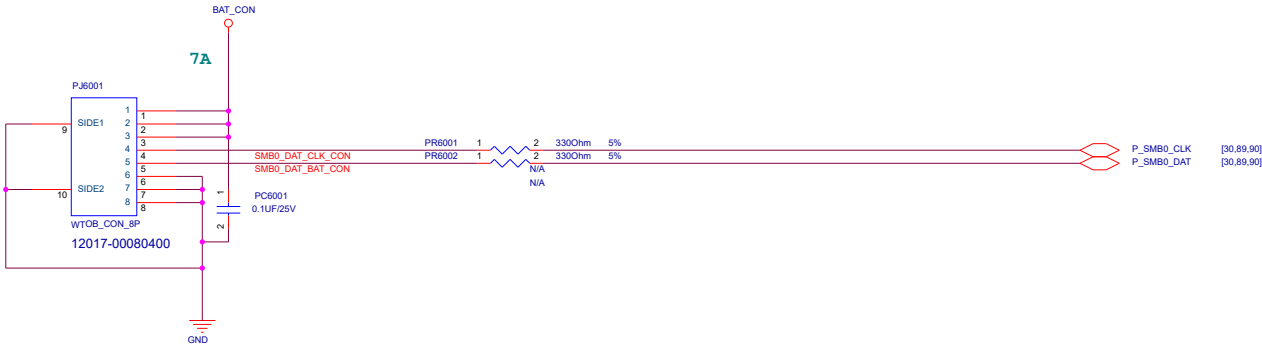
12033-00020300

J6001	3.4CH	1.55CH
	12033-00020200	12033-00020300

Main Board

Mode	ADP_INSERT_NG#	AC_IN_OC#
AC Mode	0 (POP,throttling, stop charging)	0
	1	

Battery Connector



Note:Battery Connector 正確性與BAT1_IN_OC#是否預留!

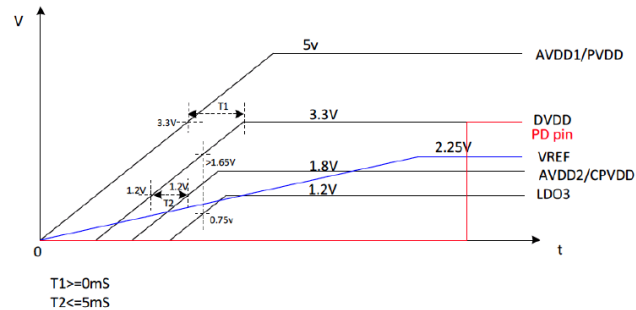
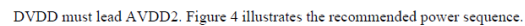
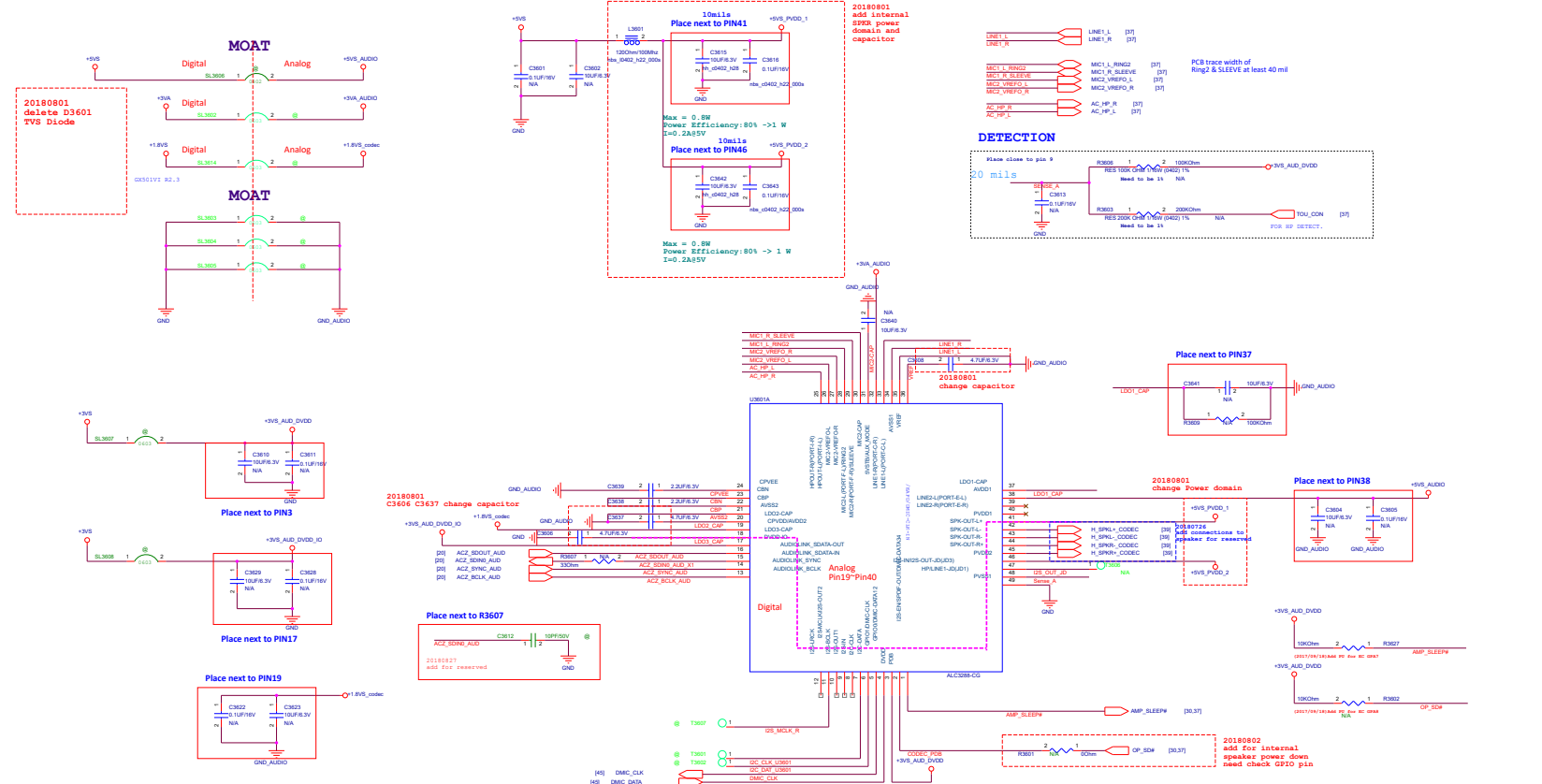
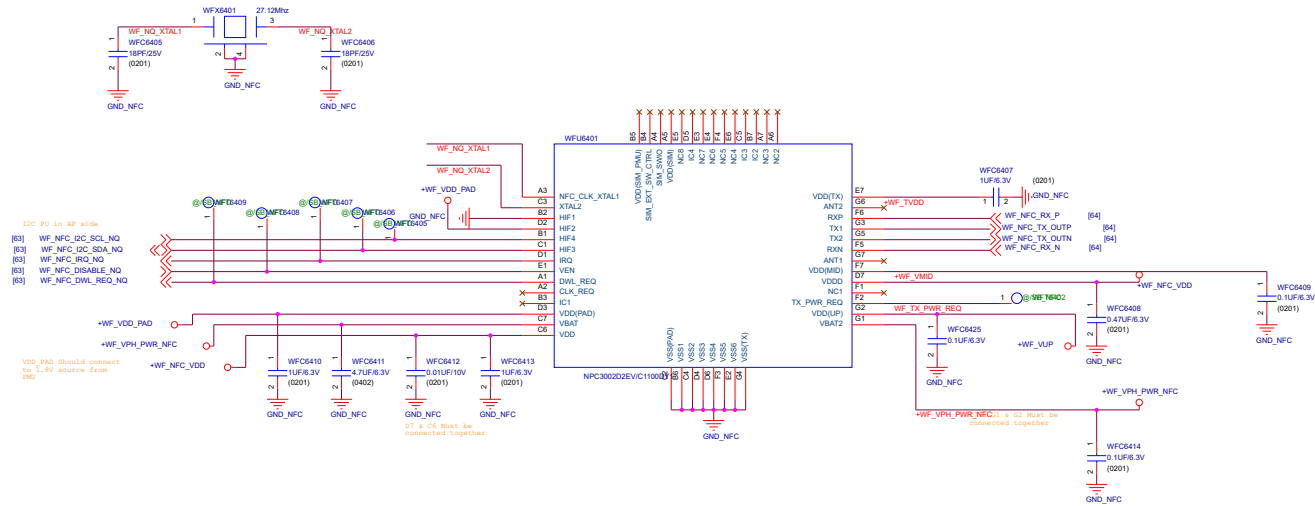
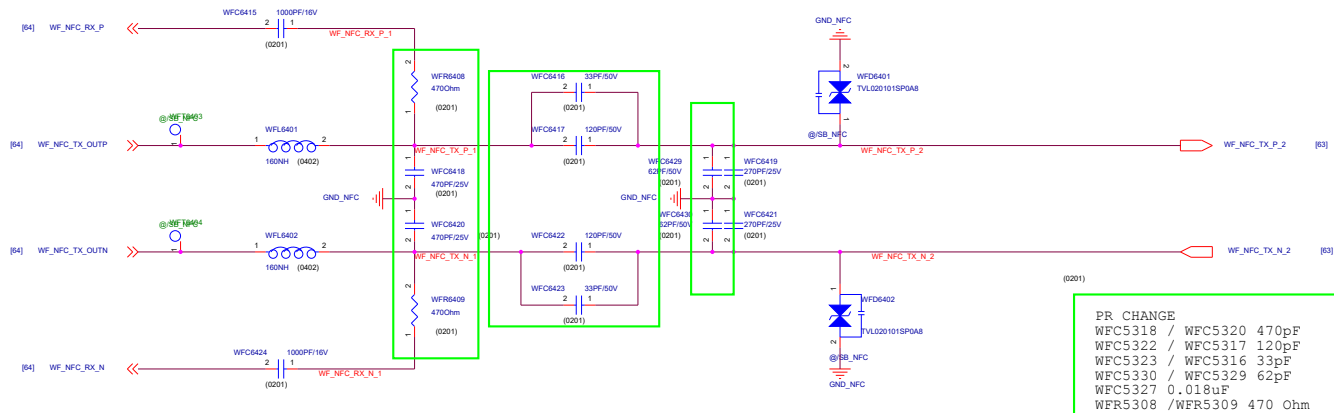


Figure 4. Power sequence



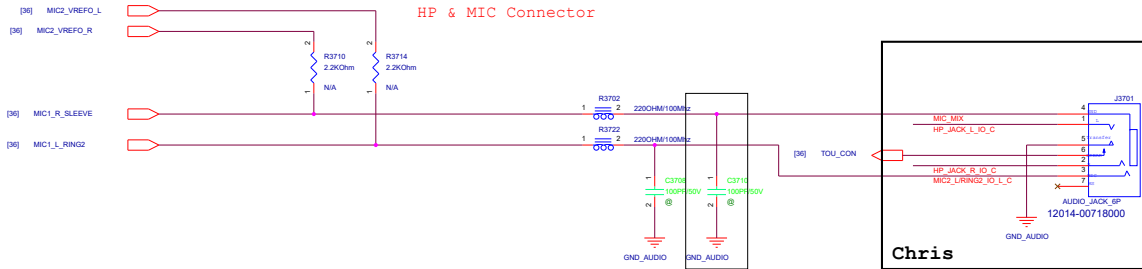
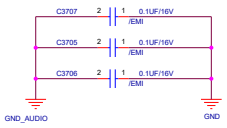
NFC Matching



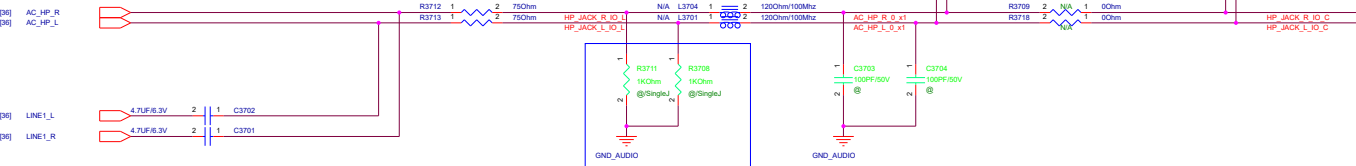
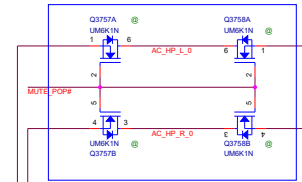
PR CHANGE
WFC5318 / WFC5320 470pF
WFC5322 / WFC5317 120pF
WFC5323 / WFC5316 33pF
WFC5330 / WFC5329 62pF
WFC5327 0.018uF
WFR5308 / WFR5309 470 Ohm

<Variant Name>

A_GND / GND



2016.09.06 Add DEPOP solution



2015.04.14 3 pole mic design and VBI2 Reserve

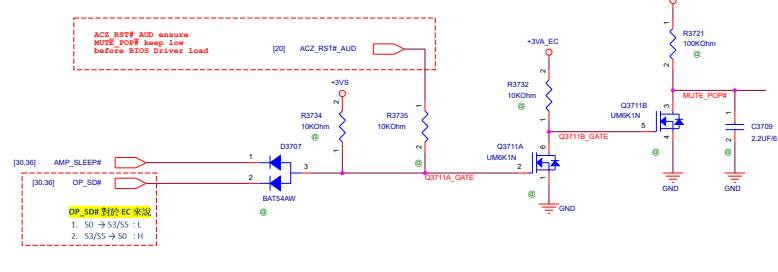
2015.08.07 Realtek Suggest

MUTE CONTROL

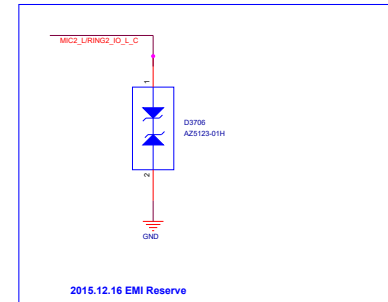
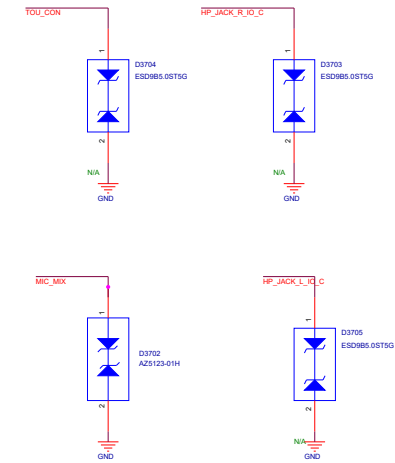
2017.03.23 AMP Change Remove

MUTE CONTROL new solution for 1.8V HDA BUG 0318

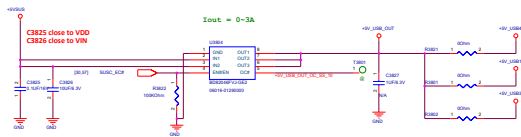
2016.07.22 Reserver DEPOP solution



HP ESD Protect



2015.12.16 EMI Reserve



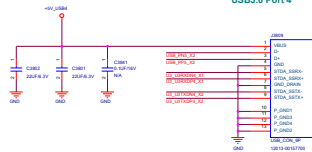
Chris

USB3.0_PORT4 (Support USB Charge Circuit)

USB3.0 Connector
1st Source: P/N: 12813-0018309 FORCONNUEA7111-B-04862-7H
2nd Source: P/N: 12813-0086408 SINGATRONZUS-0406-31610F

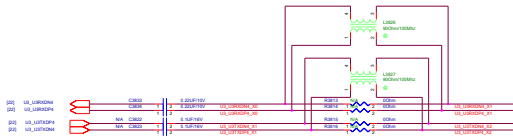
USB Charge Circuit (For PORT 4)

USB3.0 Port 4



USB3.0_PORT4

USB3.0 Pin define	
1-	VBUS-
2-	D-
3-	D+
4-	GND-
5-	RX-
6-	RX+
7-	GND-
8-	TX-
9-	TX+



USB3.0 ESD-Protection



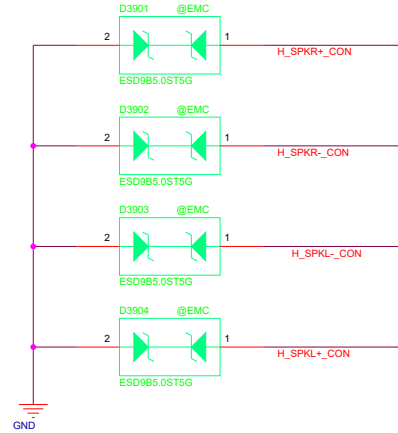
1st : 07G028076030
ESD PROTECTION AZ1045-04F
2nd : 07G028133016
ESD PROTECTION IP4284CZ10-T8

D1882 ESD Diode
1st Source: P/N:07024-0020209 AMAZINGAZC099-04SPJTG
2nd Source: P/N:07024-00710009 NXP/USB2K40

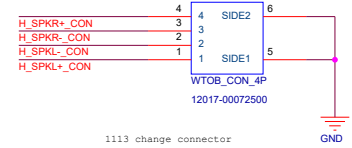
Company Name




SPK L+ L- R+ R- trace width
Speaker 8 ohm ==> 30 mils



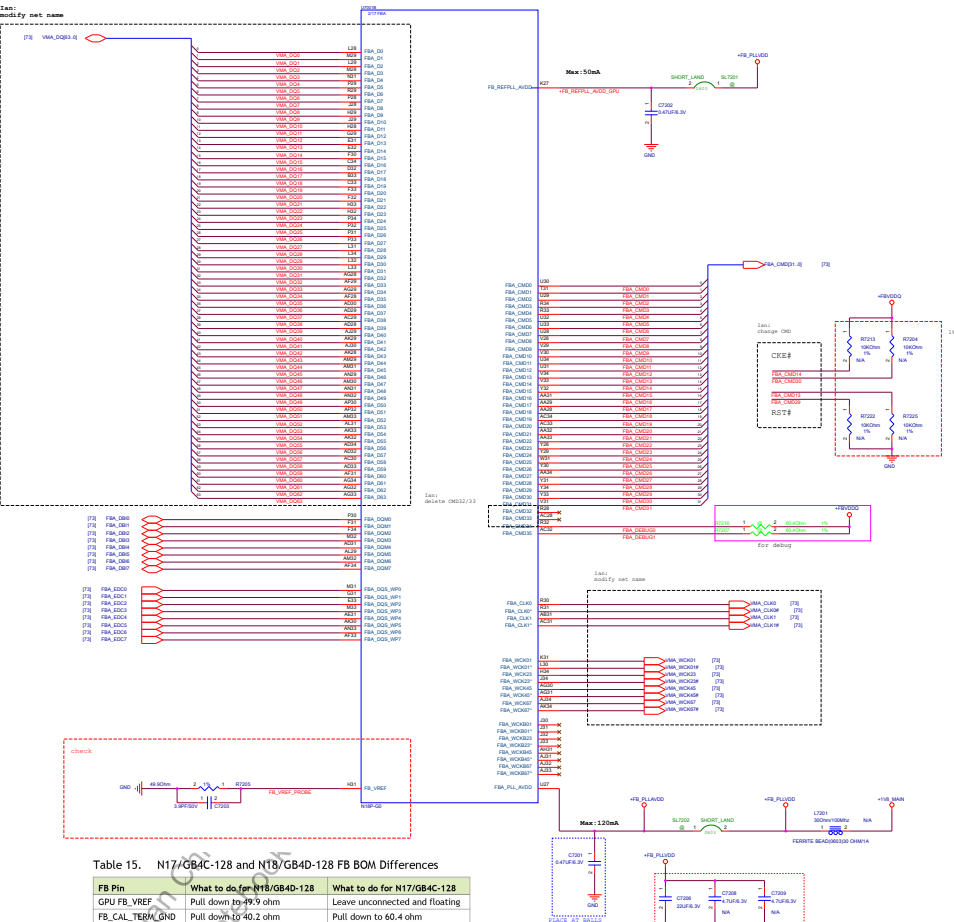
Speaker = 1.5W / channel



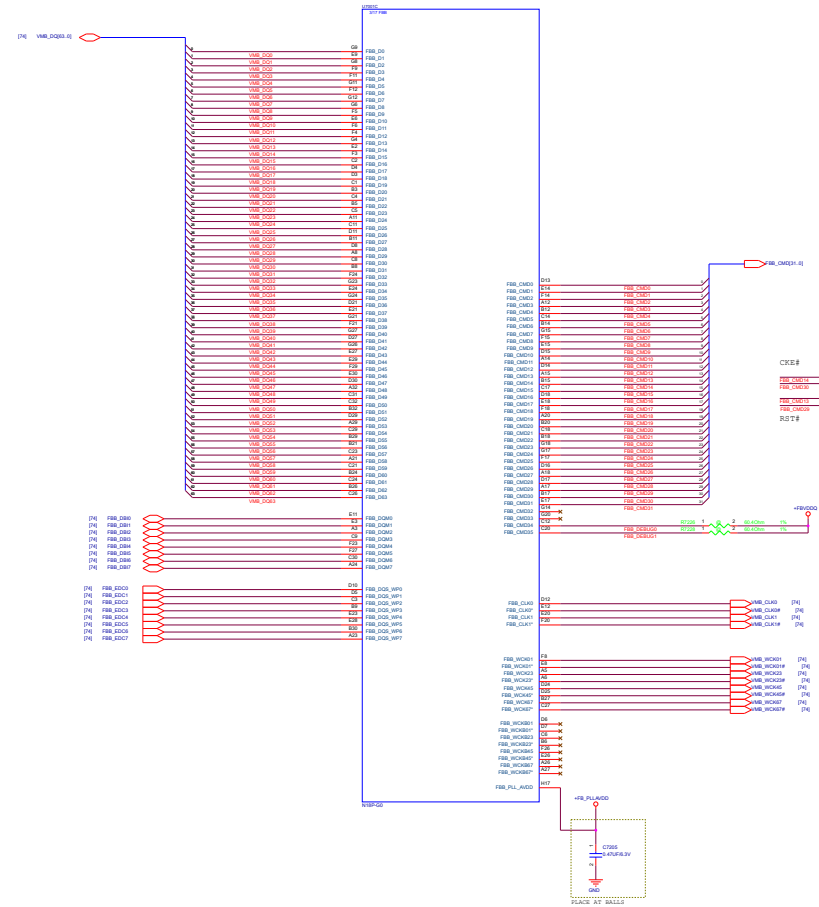
<Variant Name>

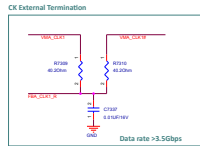
		Title : I/O board FUNC key	
ASUSTeK COMPUTER		Engineer:	Gaming RD
Size E	Project Name G711GW		Rev 1.0
Date: Tuesday, March 19, 2019		Sheet	67 of 103

MEMORY: GPU FB Partition A

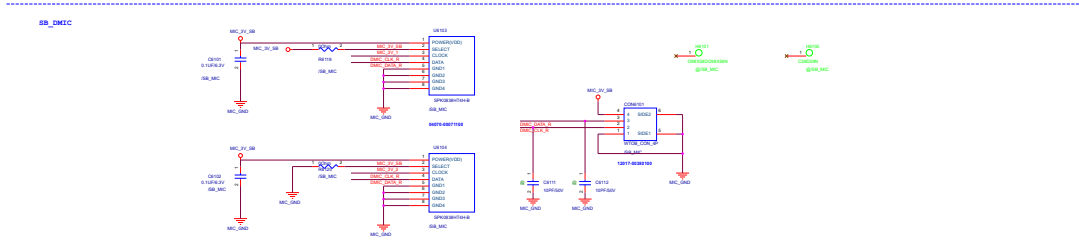


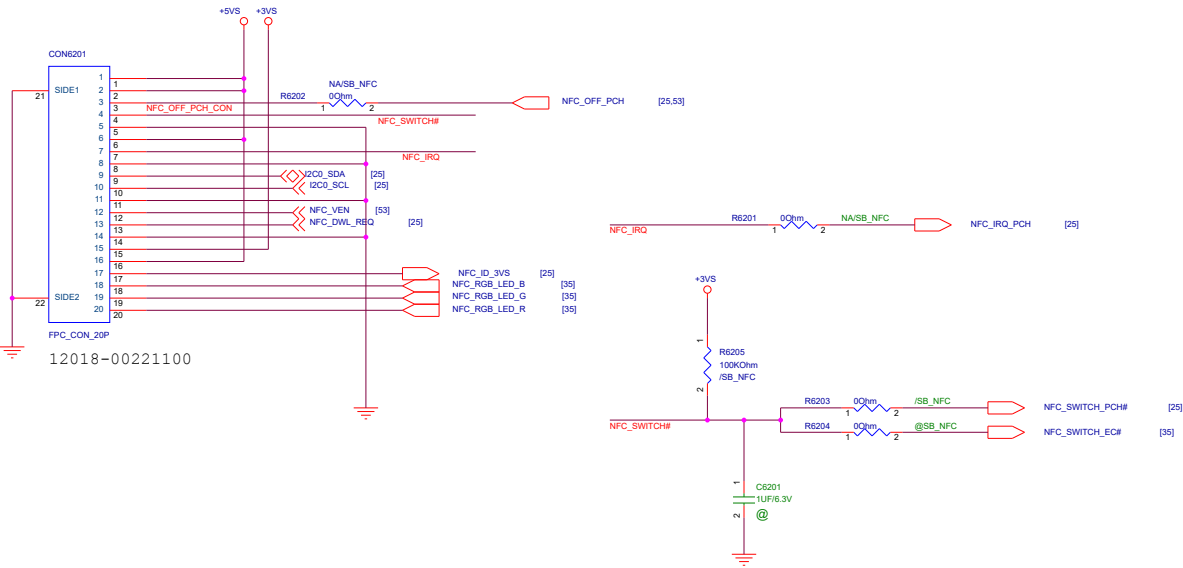
MEMORY: GPU FB Partition B



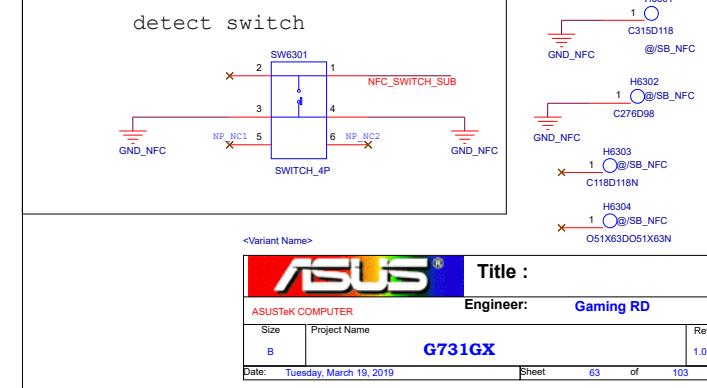
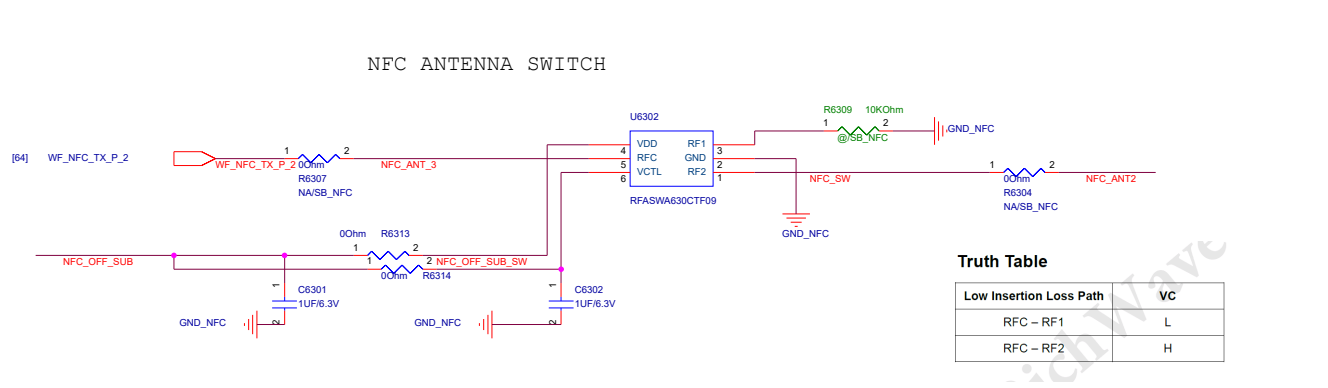
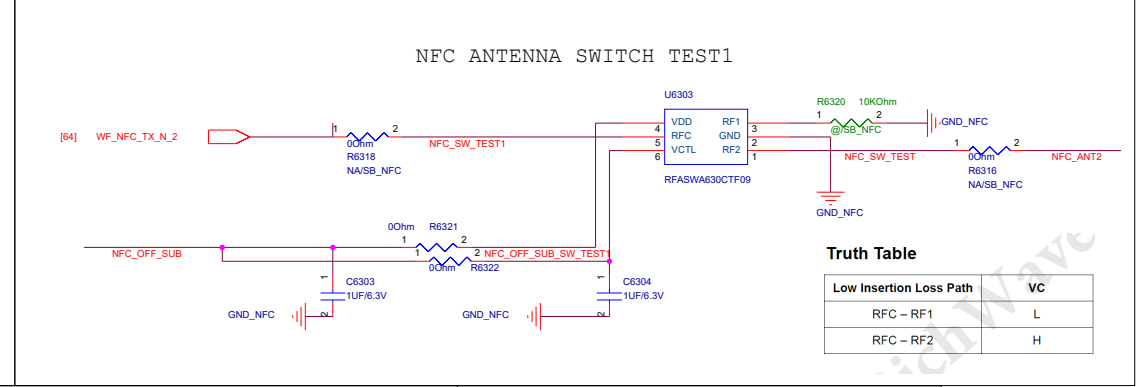
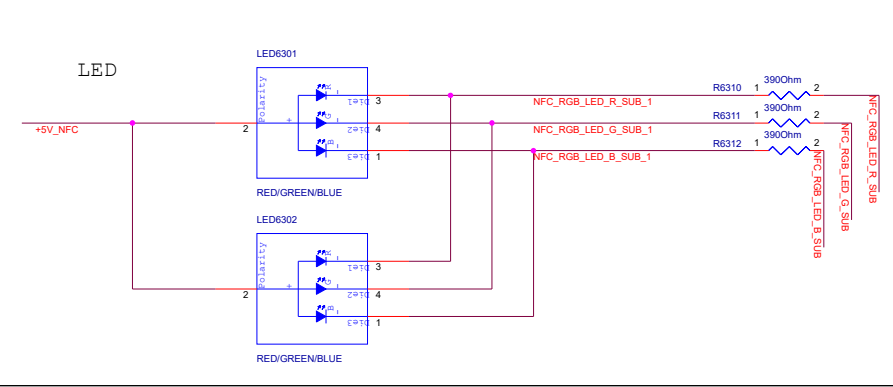
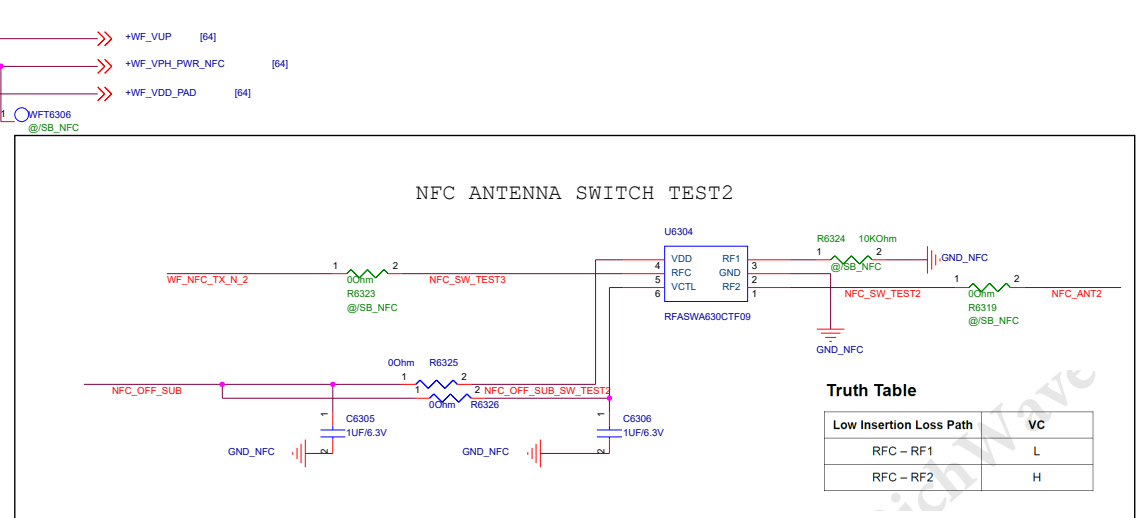
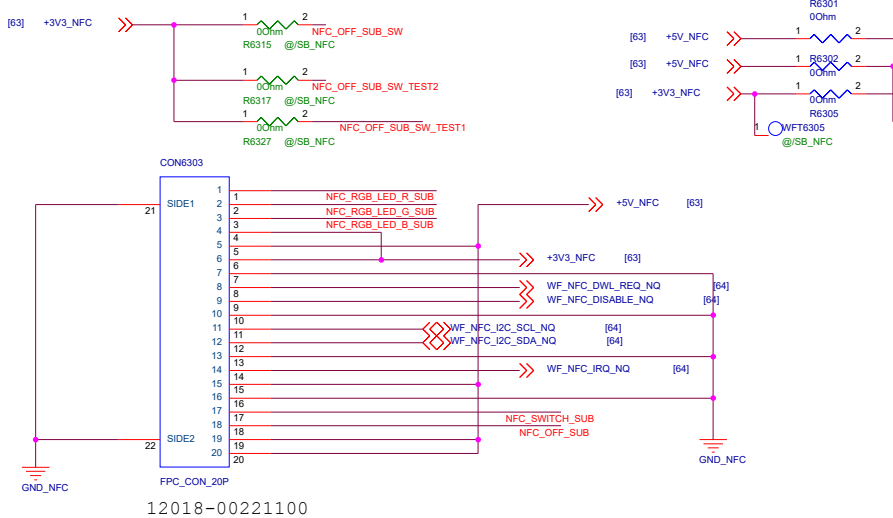
Table 4. N18P-G0 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBDV/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Part	Status
8 Gb	256Mb32	1.35 V and 1.5V ²	Micron	MT51J256M32HF-80:B	B-die	0x1	8 Gbps	N/A	Full	Production candidate
			Hynix	H5GCH2H44LR-82C	A-die	0x2	8 Gbps	N/A	Full	Production candidate
		1.35V and 1.55V ²	Samsung	K4G803225FC-HC25	C-die	0x0	8 Gbps ²	N/A	Full	Production candidate





<Variant Name>

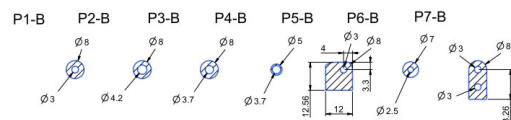


Truth Table	
Low Insertion Loss Path	VC
RFC – RF1	L
RFC – RF2	H

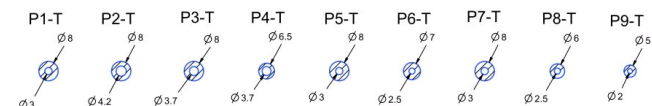
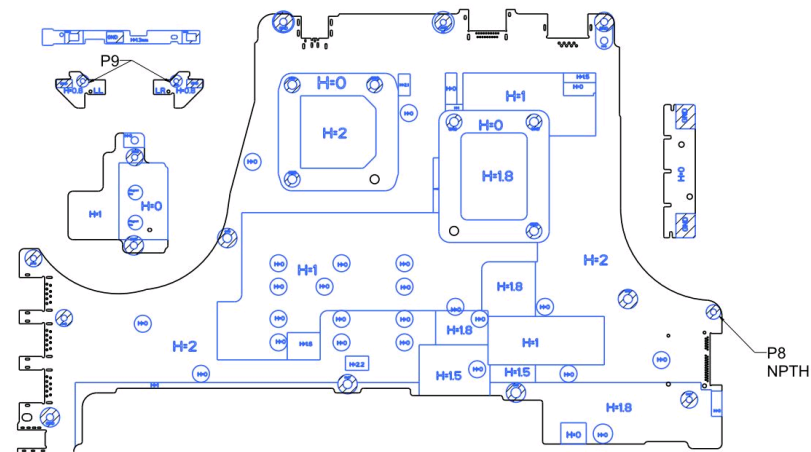
Truth Table	
Low Insertion Loss Path	VC
RFC – RF1	L
RFC – RF2	H

Truth Table	
Low Insertion Loss Path	VC
RFC – RF1	L
RFC – RF2	H

[TOP](#)



[TOP](#)



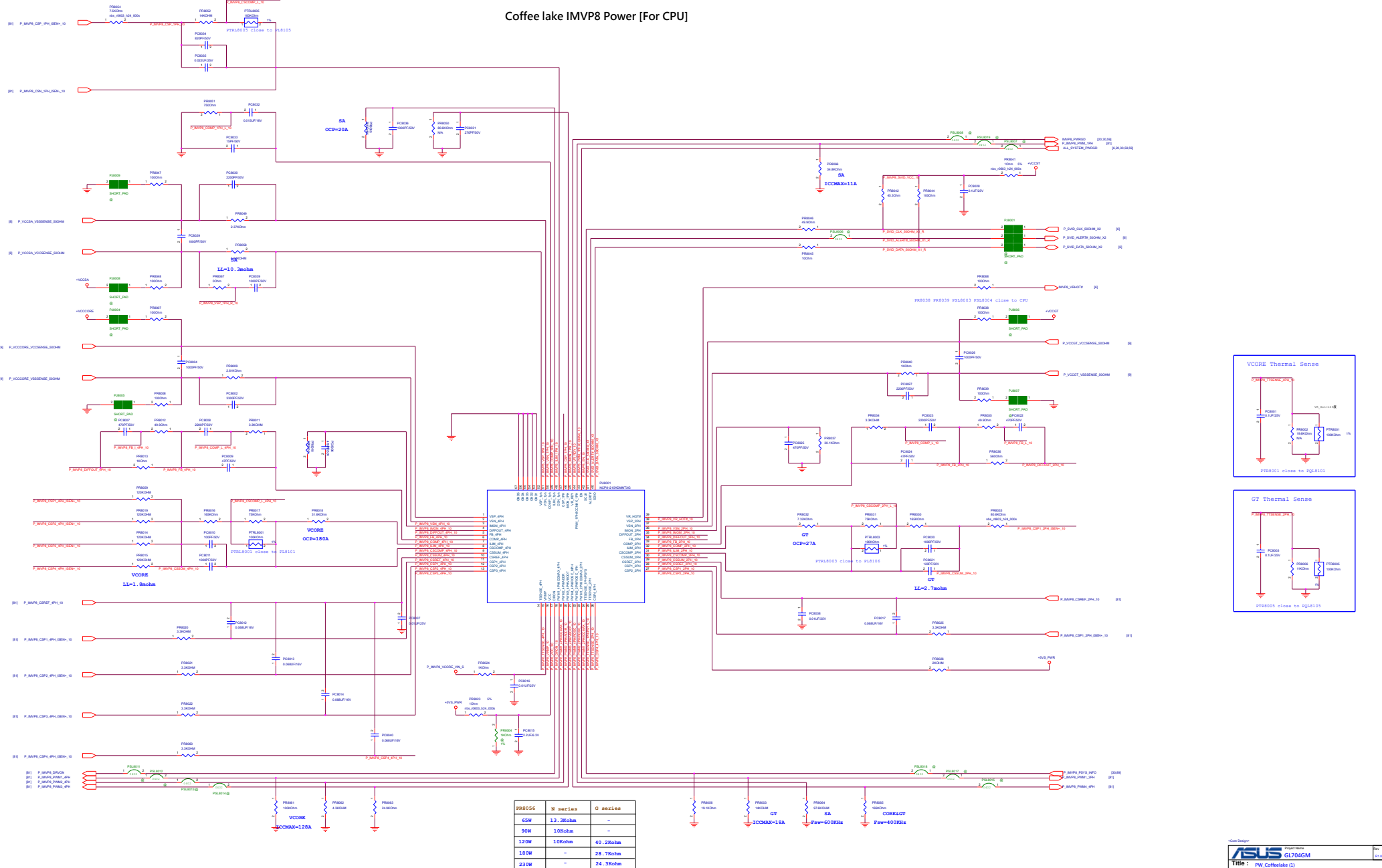
Technical drawing of a mechanical part, likely a bracket or support, showing dimensions R1.5 and 4. The drawing includes a cross-section view and a side view. The cross-section view shows a rectangular profile with rounded corners (R1.5) and a central hole. The side view shows the part's profile with a central hole and a flange. The dimension 4 indicates the width of the part.

Technical drawing of a mechanical part. A red box highlights a feature with dimensions $\phi 2.5$ and $\phi 6$. The text **NPTH** is written in red above the box. Other dimensions shown are $\phi 3.7$ and $\phi 8$.

Technical drawing of a staircase showing a side elevation and a plan view. The side elevation shows a staircase with a vertical rise of $H=0.9$ and a horizontal run of $H=0.6$. The plan view shows a staircase with a vertical rise of $H=1.7$ and a horizontal run of $H=1.7$. The drawing includes dimensions for the steps and the overall height and width of the staircase.

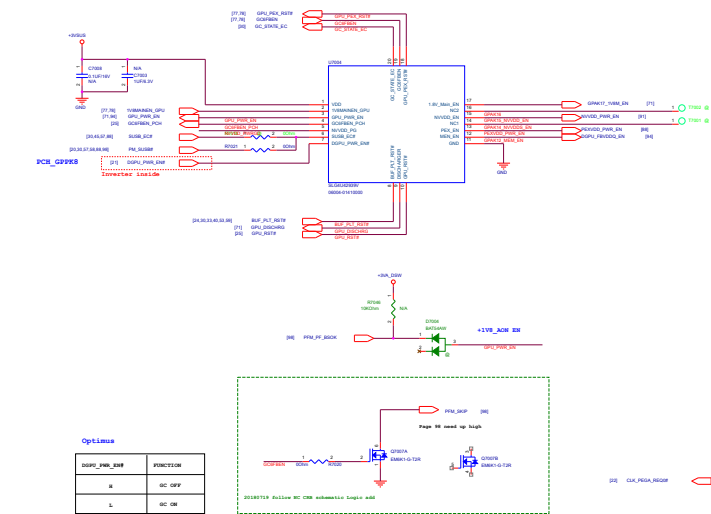
Technical drawing of a mechanical part. The drawing shows a cross-section of a component with a central hole. The outer diameter is labeled $\varnothing 8$. The inner hole diameter is labeled $\varnothing 3$. A label 'NPTH' (Not Plated Through) points to the outer edge of the part. A blue circle with an arrow indicates a specific feature or direction.

Coffee lake IMVP8 Power [For CPU]



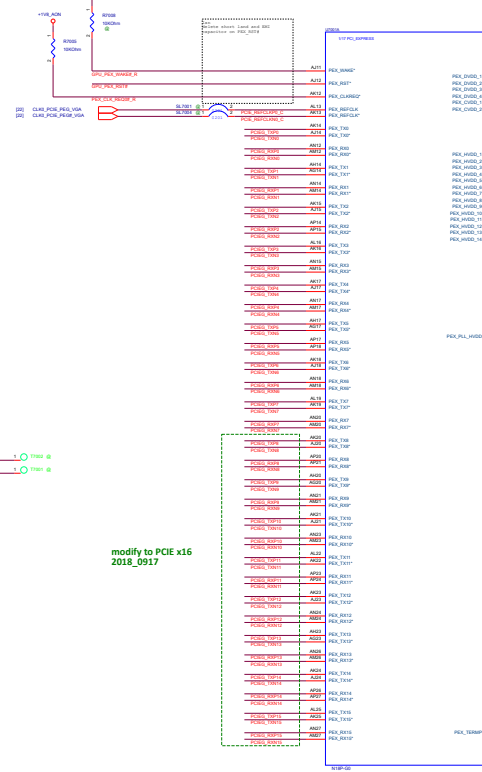


GPU POWER SEQUENCE CONTROL



DGPO_FWR_EN#	FUNCTION
H	GC OFF
L	GC ON

PCI EXPRESS_Graphics
REVERSED Type PCIE X16



modify to PCIe x16
2018_0917

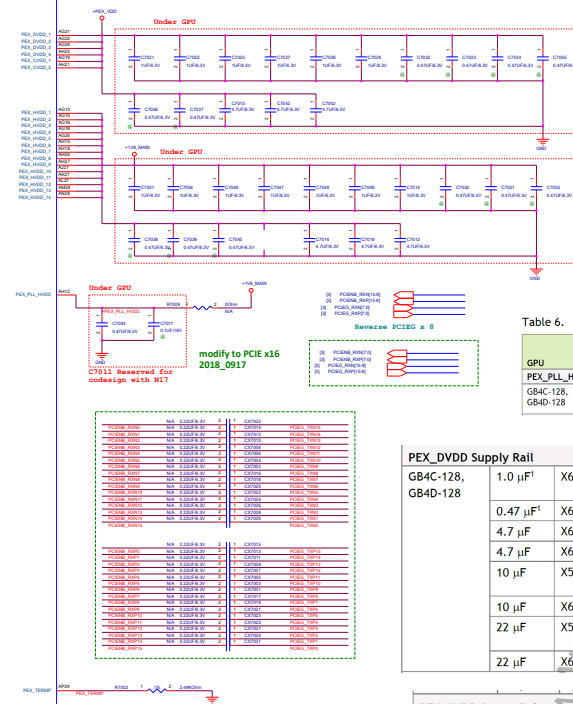


Table 6. PEX PLLs Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population		Location	
			N18	N17		
PEX_PLL_HVDD Supply Rail						
GB4C-128;	0.1 μ F	X7R	0402	0	1	Under GPU
GB4D-128	0.47 μ F ¹	X6S	0201W	1	0	Under GPU

PEX_DVDD Supply Rail

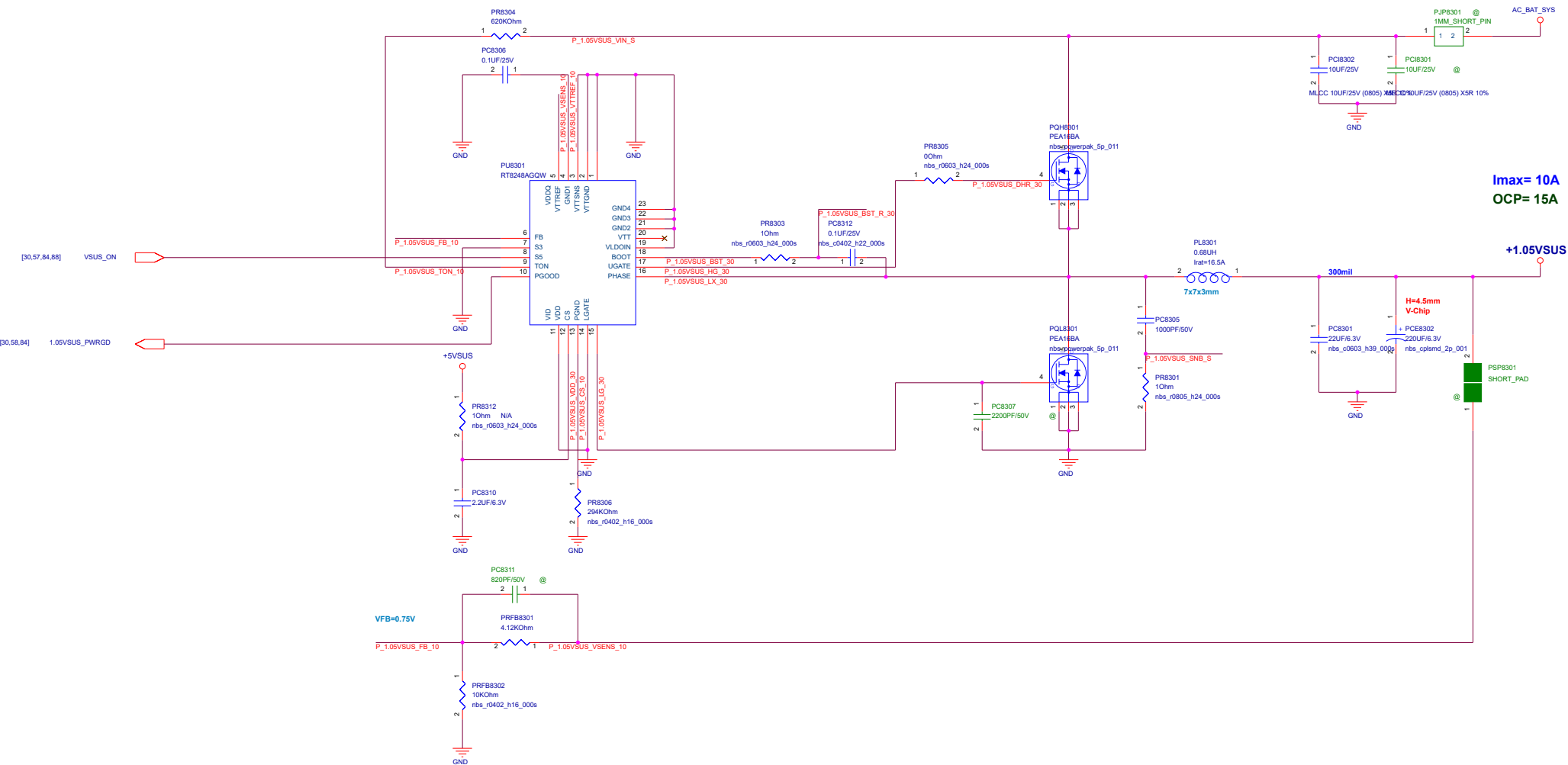
GB4C-128, GB4D-128	1.0 μF^\dagger	X6S	0402 or 0201W	0	4	Under GPU
	0.47 μF^\dagger	X6S	0201W	12	0	Under GPU
	4.7 μF	X6S	0603	0	2	Near GPU
	4.7 μF	X6S	0603	3	0	Under GPU
	10 μF	X5R	0805	0	1	Midway between GPU and power supply
	10 μF	X6S	0805	3	0	Near GPU
	22 μF	X5R	0805	0	1	Midway between GPU and power supply
	22 μF	X6S	0805	2	0	Near GPU

PEX_HVDD Supply Rail	
----------------------	--

GB4C-128, GB4D-128	1.0 μF	X6S	0402 or 0201W	0	4	Under GPU
	0.47 μF	X6S	0201W	13	0	Under GPU
	4.7 μF	X6S	0603	0	2	Near GPU
	4.7 μF	X6S	0603	3	0	Under GPU
	10 μF	X5R	0805	0	2	Midway between GPU and power supply
	10 μF	X6S	0805	3	0	Near GPU
	22 μF	X5R	0805	0	1	Midway between GPU and power supply
	22 μF	X6S	0805	2	0	Near GPU

modify to PCIE x16
2018_0716

+1.05VSUS [For PCH]

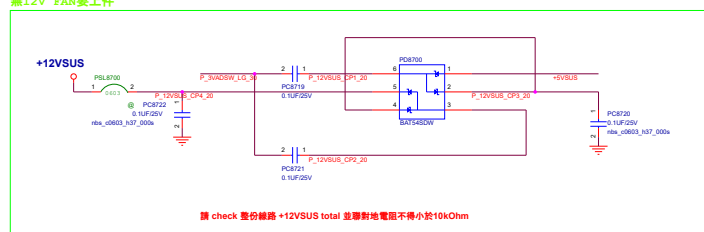


Imax= 10A
OCP= 15A

+1.05VSUS

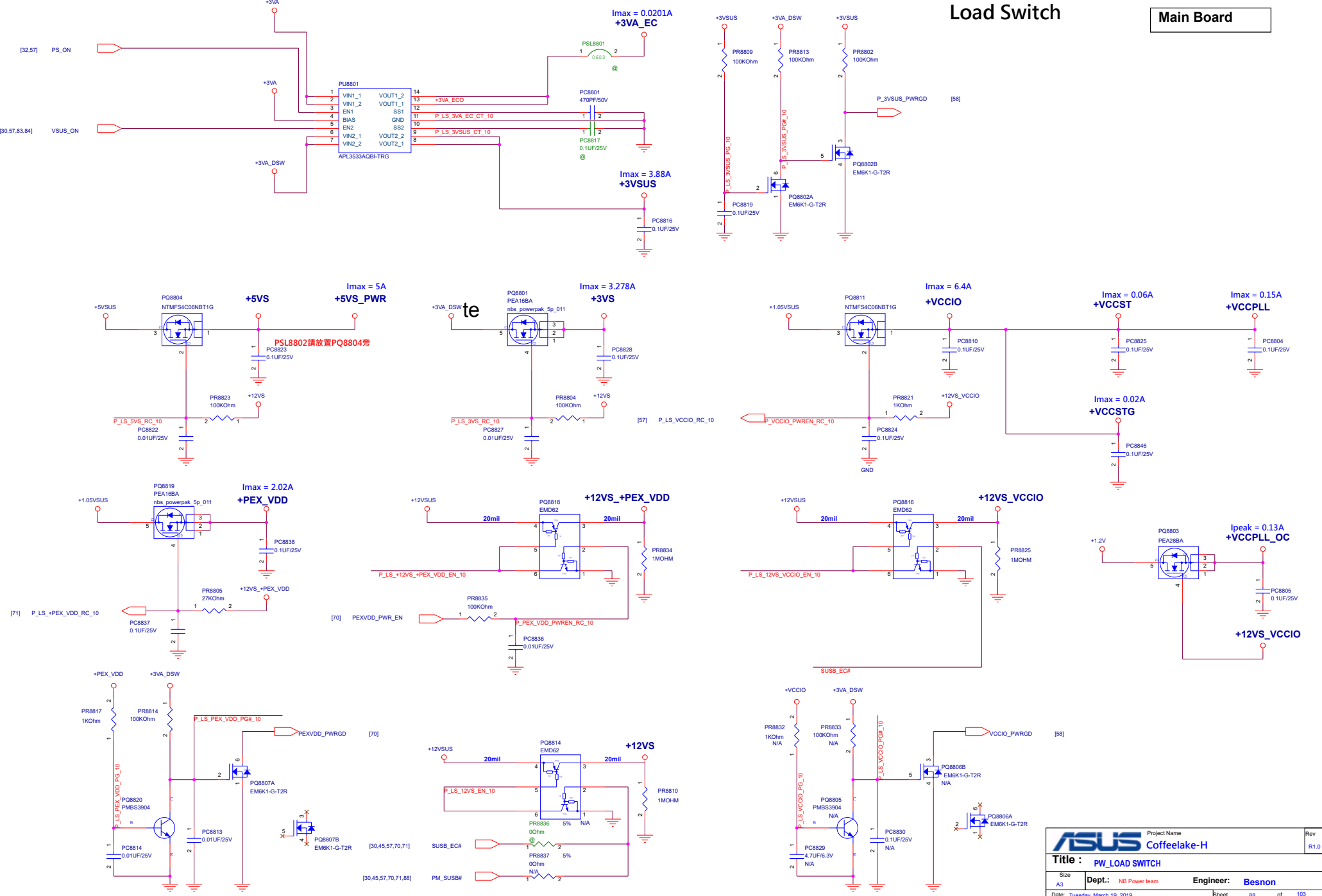
PT830* 請放置 PU8301旁;並請放置Trace上!

P_1.05VSUS_HG_30 @
P_1.05VSUS_LX_30 @
P_1.05VSUS_LG_30 @

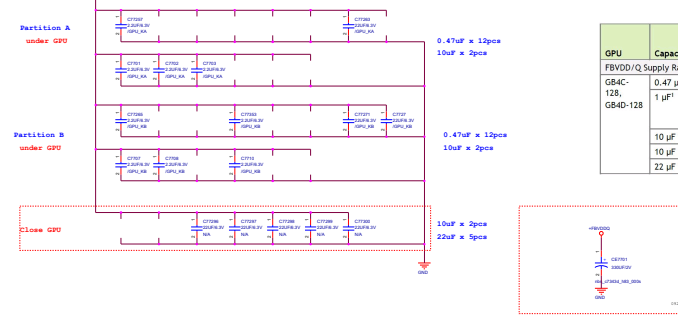


Load Switch

Main Board

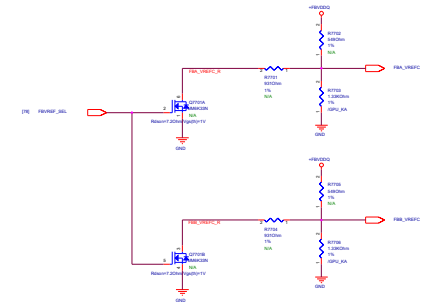
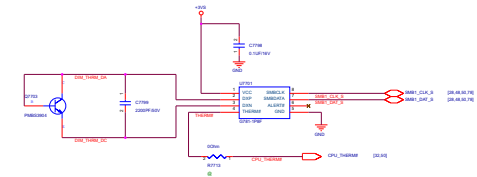


VRAM_PWR_FBVDDQ



The diagram shows a 330uF 10V electrolytic capacitor connected to a 12VDC input and ground. The capacitor is represented by two parallel lines of unequal length, with the longer line on the left. The left terminal is connected to a red wire labeled "12VDCIN". The right terminal is connected to a red wire labeled "GND". The capacitor is labeled "330uF 10V".

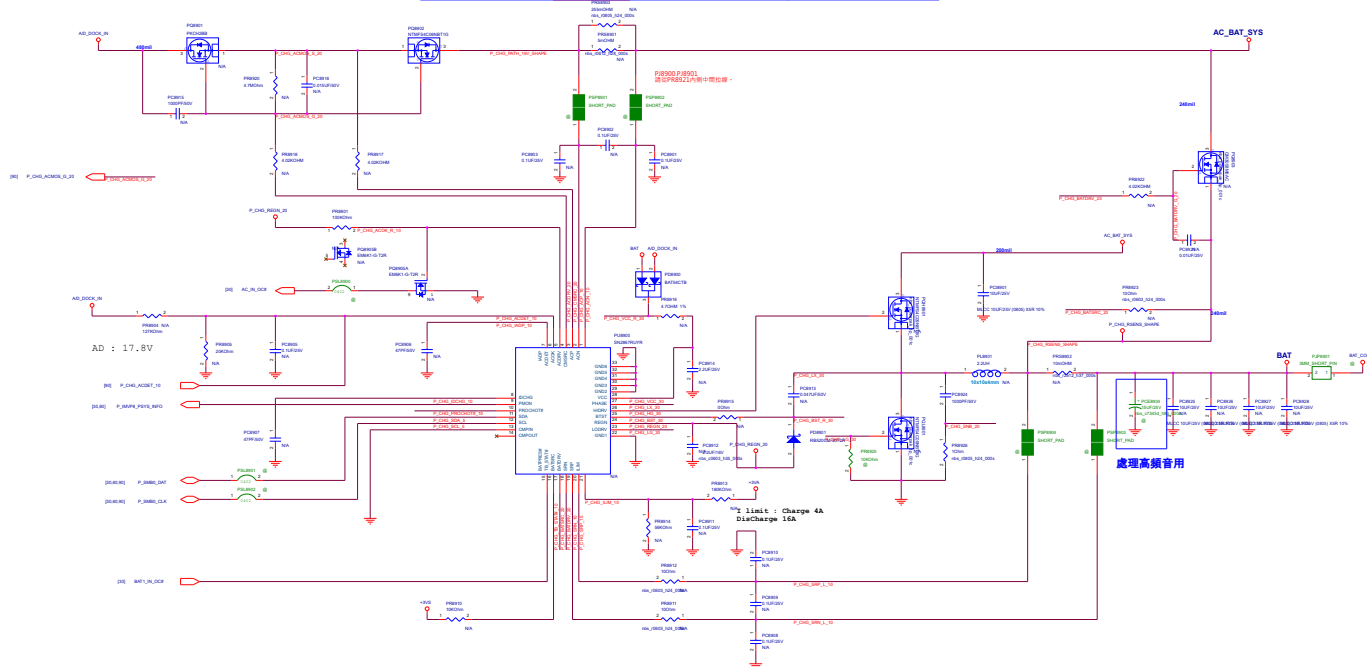
Variable	Value	Unit	Value	Unit
[0, 78]	GPU_FLEX_RATE	1	0.0000	0.0000
[1, 78]	TSVMANMAN_GPU	1	0.0000	0.0000
[2, 78]	GOFORM	1	0.0000	0.0000
[30, 78, 78]	DGPU_PWDKX	1	0.0000	0.0000
[38, 78]	GPUVENTATE_PCH	1	0.0000	0.0000



		Project Name	Rev
Title : YARM		G731GX	Rev 1
Drawn	Dapt.:	Engineer:	
AD	ASUS/MS COMPUTER	Gaming RD	
Date: Sunday, March 18, 2018		Sheet	77 of 103

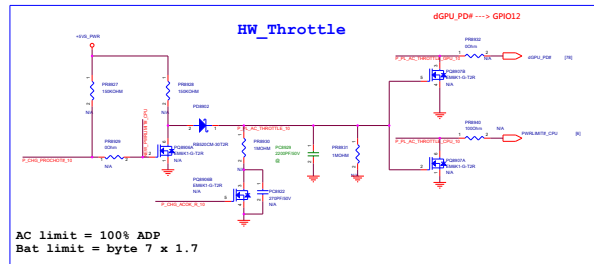
PR8901	ADP<120W	ADP<230W	ADP<230W	ADP<330W		
	TSD		5m	2m		
	YES	YES/NO-OTHERS	YES/NO-OTHERS	YES/NO-OTHERS		

PR8903	ADP=120W	ADP=150W	ADP=180W	ADP=230W	ADP=280W	ADP=330W
	200m	255m	X	X	X	560m
	YES/NO-OTHERS	YES/NO-OTHERS	X	X	X	YES/NO-OTHERS

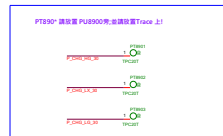


Adaptor select
total power = 90% ADP

Adaptor select				
		M Series	D Series	
PR8921		10m	5m	
PR8936				
14K	0.4V	30W	120W	
31.6K	0.8V	40W	150W	
56K	1.2V	45W	180W	
93.1K	1.6V	65W	230W	
150K	2.0V	75W	280W	
270K	2.4V	90W	330W	
560K	2.8V	120W	400W	

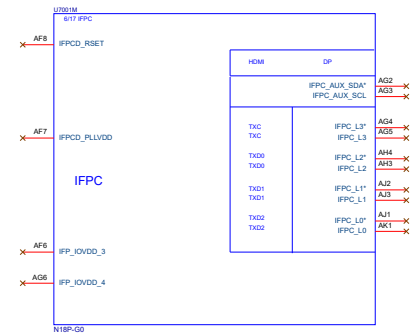
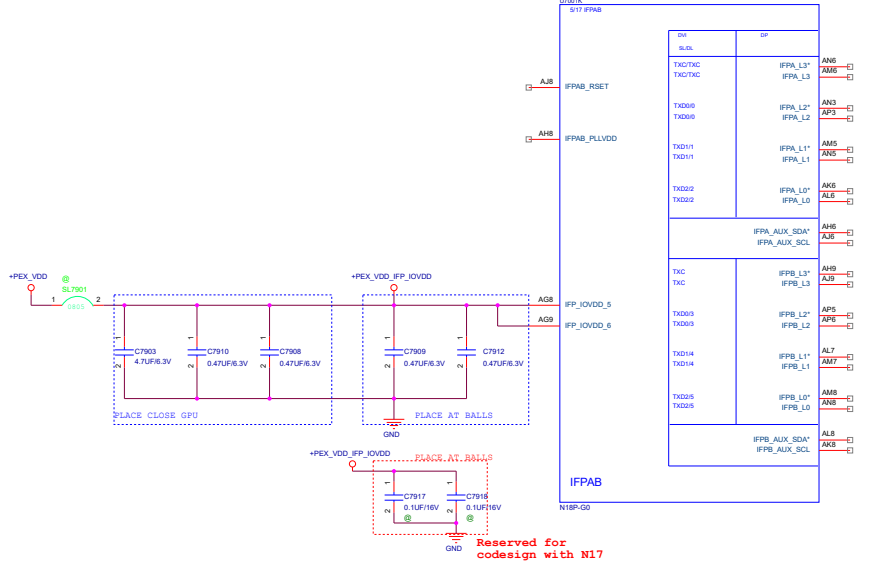


AC limit = 100% ADP
Bat limit = byte x 1.7

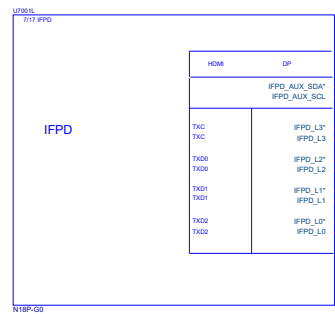


Project Name		File
Coffee lake-H		File
Title		File
PK CHARGER		File
Author		File
Engineer		File
Date		File
Page		File
Total		File

DP (Type-C)

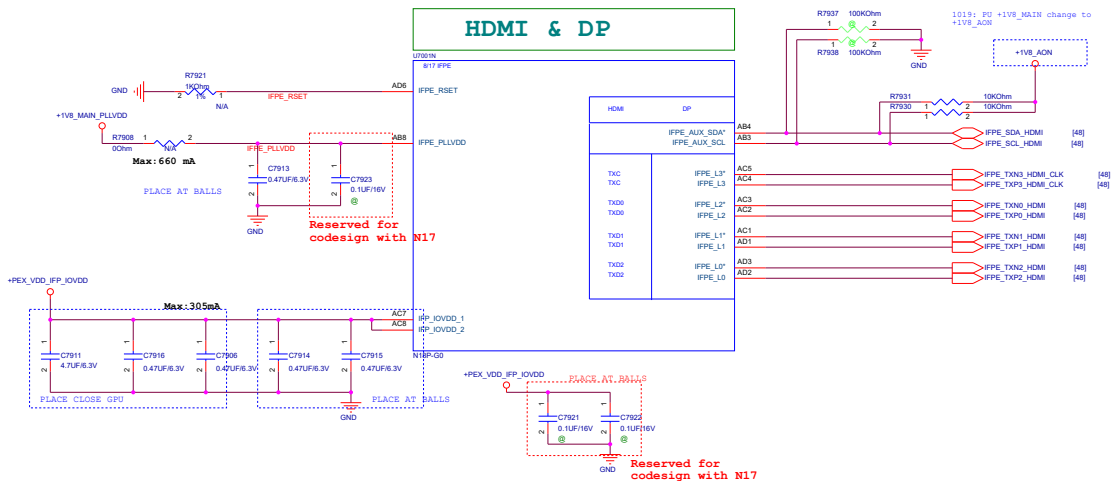
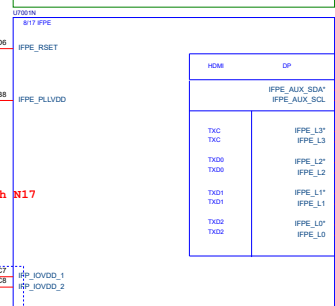


EDP (4Lane Panel)



Chris

HDMI & DP



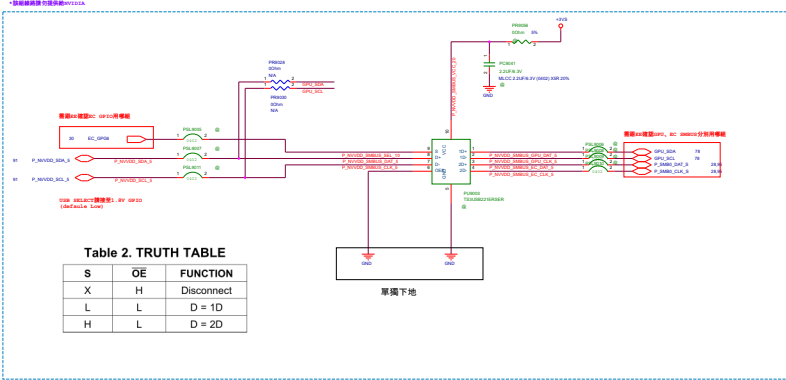
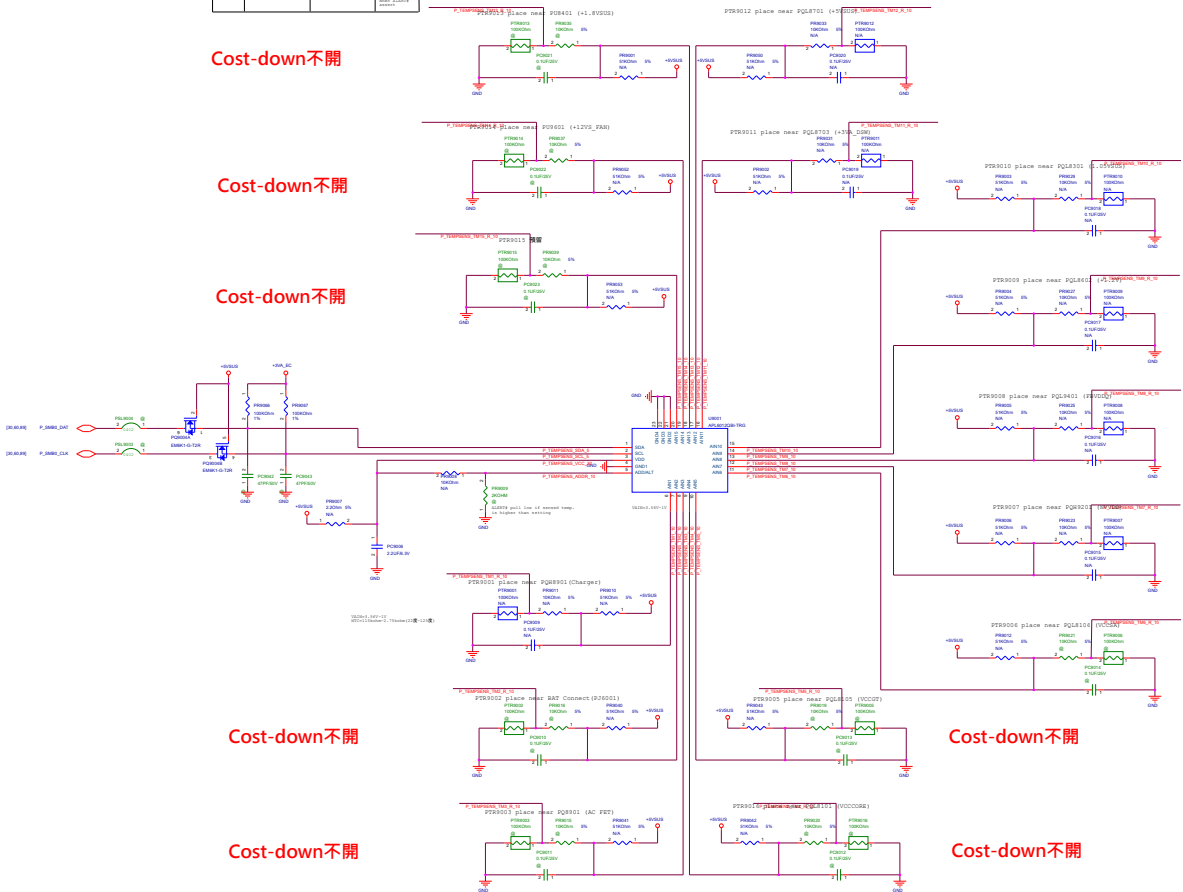
GPU	Type	Footprint	Population		Location
			N18	N17	
IFP_IOVDD Supply Rails					
GB4C-128, GB4D-128	0.1 μ F	X7R 0402	0	6	Under GPU; 1 per ball
	0.47 μ F ¹	X6S 0201W	6	0	Under GPU; 1 per ball
	1.0 μ F ²	X6S 0402 or 0201W	0	3	Near GPU
	0.47 μ F ²	X6S 0201W	6	0	Near GPU
	4.7 μ F	X6S 0603	3	3	Near GPU
	Bead Type				
	180 Ω @ 100 MHz (ESR=0.2 Ω)	0603	0	0	Near GPU

GPU	Type	Footprint	Population		Location	
			N18	N17		
IFPAB_PLLVDD Supply Rail						
GB4C-128	0.1 μ F	X7R	0402	0	1	Under GPU
GB4D-128	0.47 μ F ¹	X6S	0201W	1	0	Under GPU
Bead Type						
	300 Ω @ 100 MHz (ESR=0.25 Ω)	0603		0	0	Near GPU
N17: IFPCD_PLLVDD and IFPEF_PLLVDD Supply Rails						
N18: IFPCD_PLLVDD and IFPE_PLLVDD Supply Rails						
GB4C-128	0.1 μ F	X7R	0402	0	2	Under GPU; 1 per ball
GB4D-128	0.47 μ F ¹	X6S	0201W	2	0	Under GPU; 1 per ball
Bead Type						
	300 Ω @ 100 MHz (ESR=0.25 Ω)	0603		0	0	Near GPU

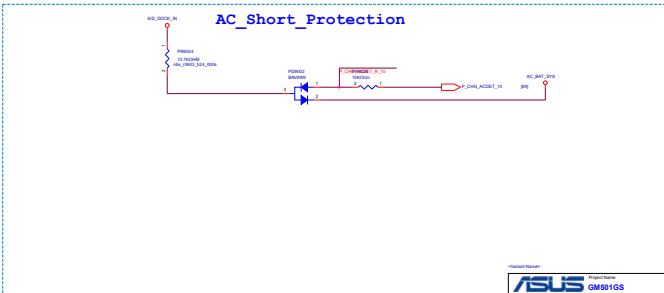
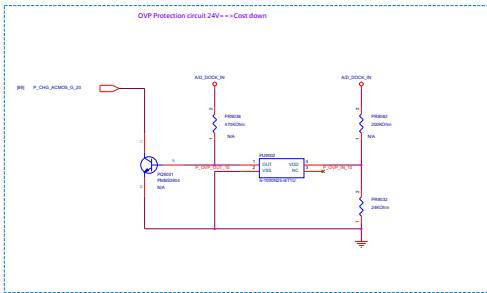
Address Selection Table											
Address	SEL1	SEL2	SEL3	SEL4	SEL5	SEL6	SEL7	SEL8	SEL9	SEL10	SEL11
0x0000	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
0x0001	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
0x0002	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0

Register Address											
Register	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
0x0000	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
0x0001	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
0x0002	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0

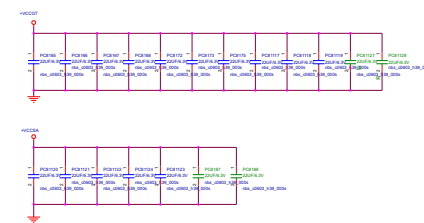
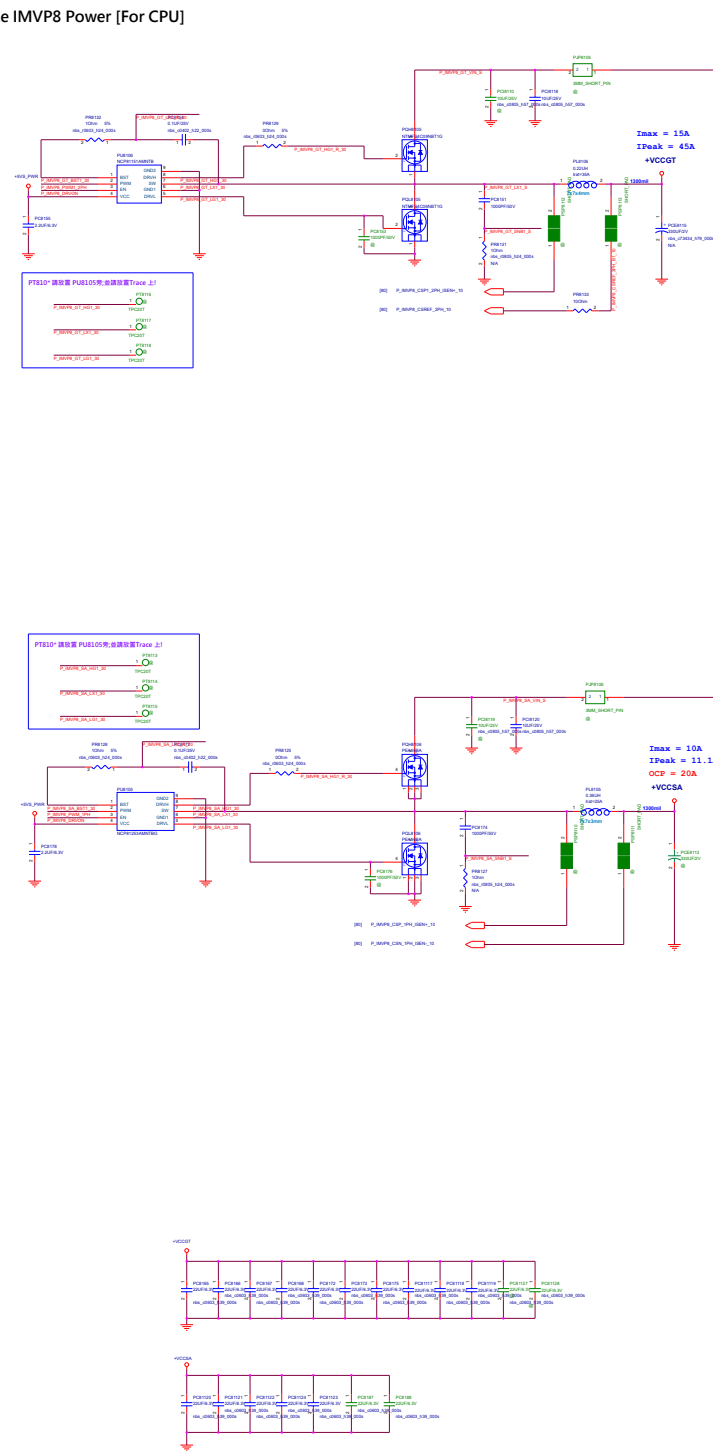
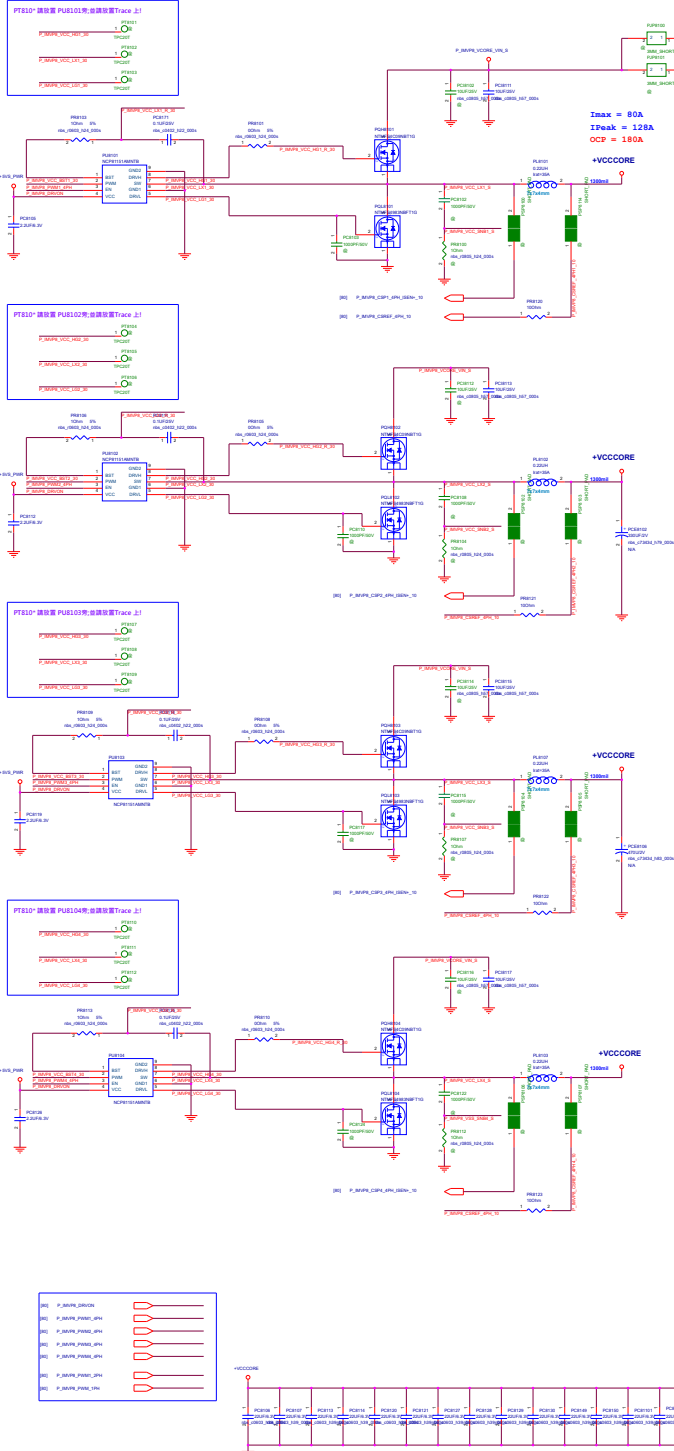
PROTECTION

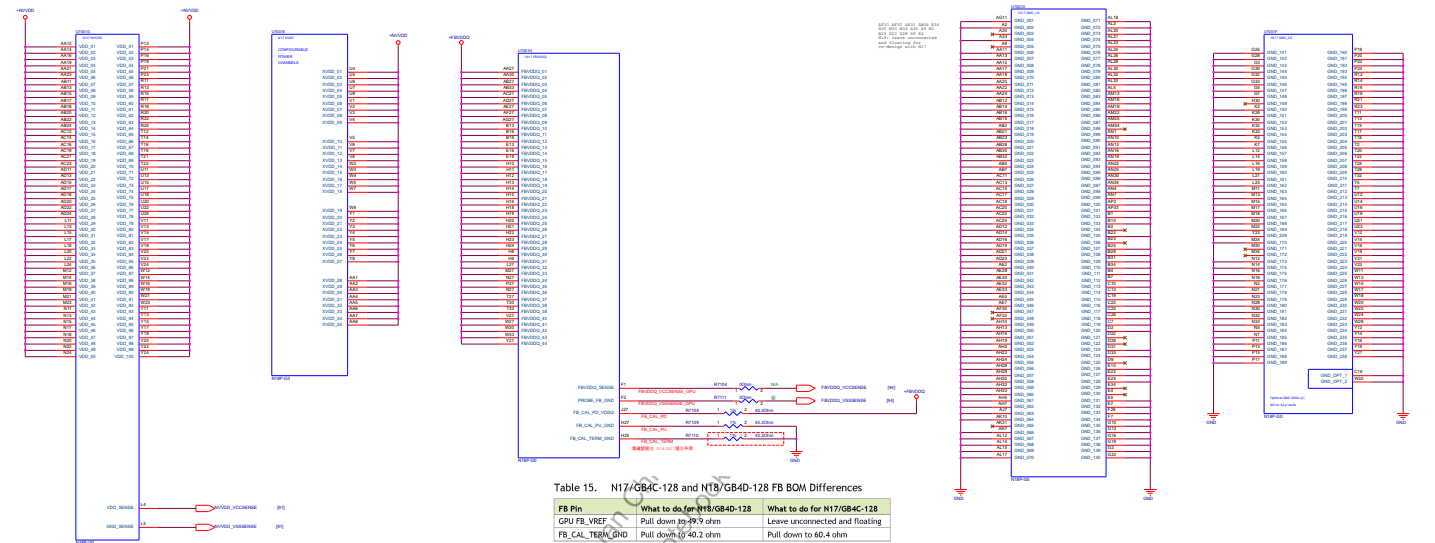


Cost-down不開



Coffee lake IMVP8 Power [For CPU]





Discharge

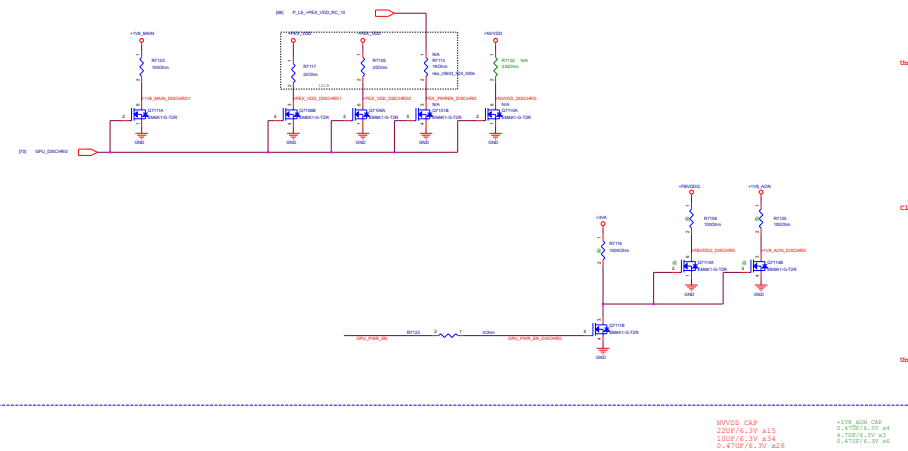


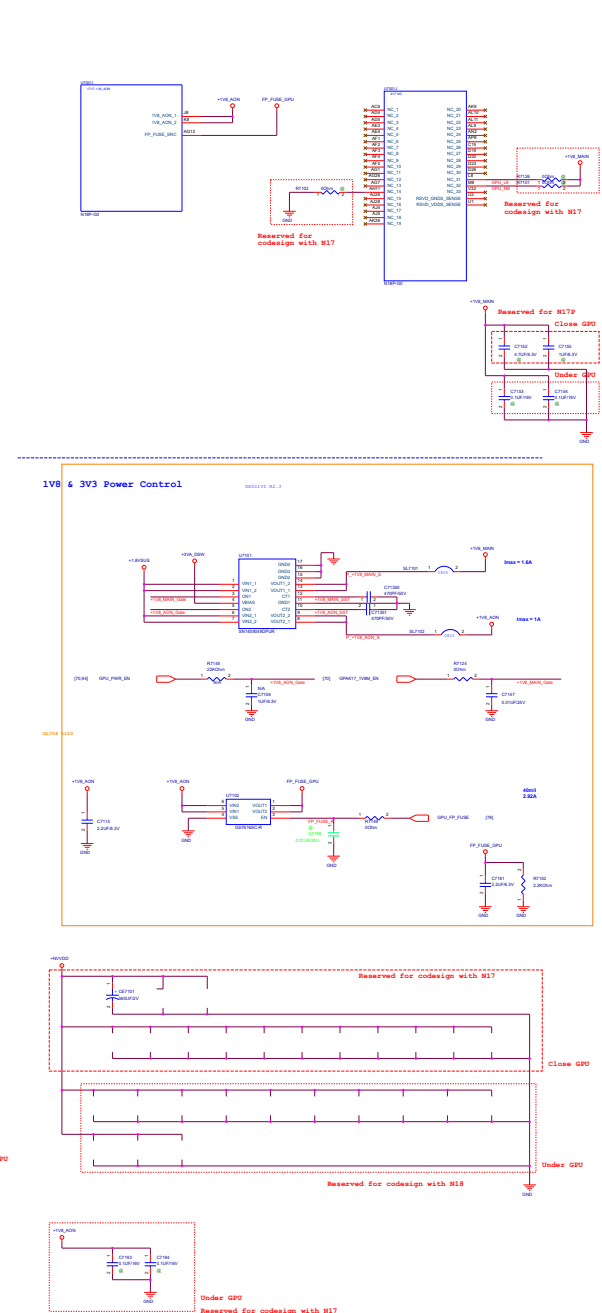
Table 2. NVVDD Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population	Location
NVVDD Supply Net				
GB4C-128,	10 μ F	X6S 0603	34	21
GB4D-128	1 μ F ¹	X6S 0402 or 0201W	0	13
	0.47 μ F ¹	X6S 0402 or 0201W	26	0
	10 μ F	X6S 0603	0	1
	22 μ F	X6S 0805	15	10
	4.7 μ F	X6S 0603	0	2
	330 μ F	POS 7343	0	1

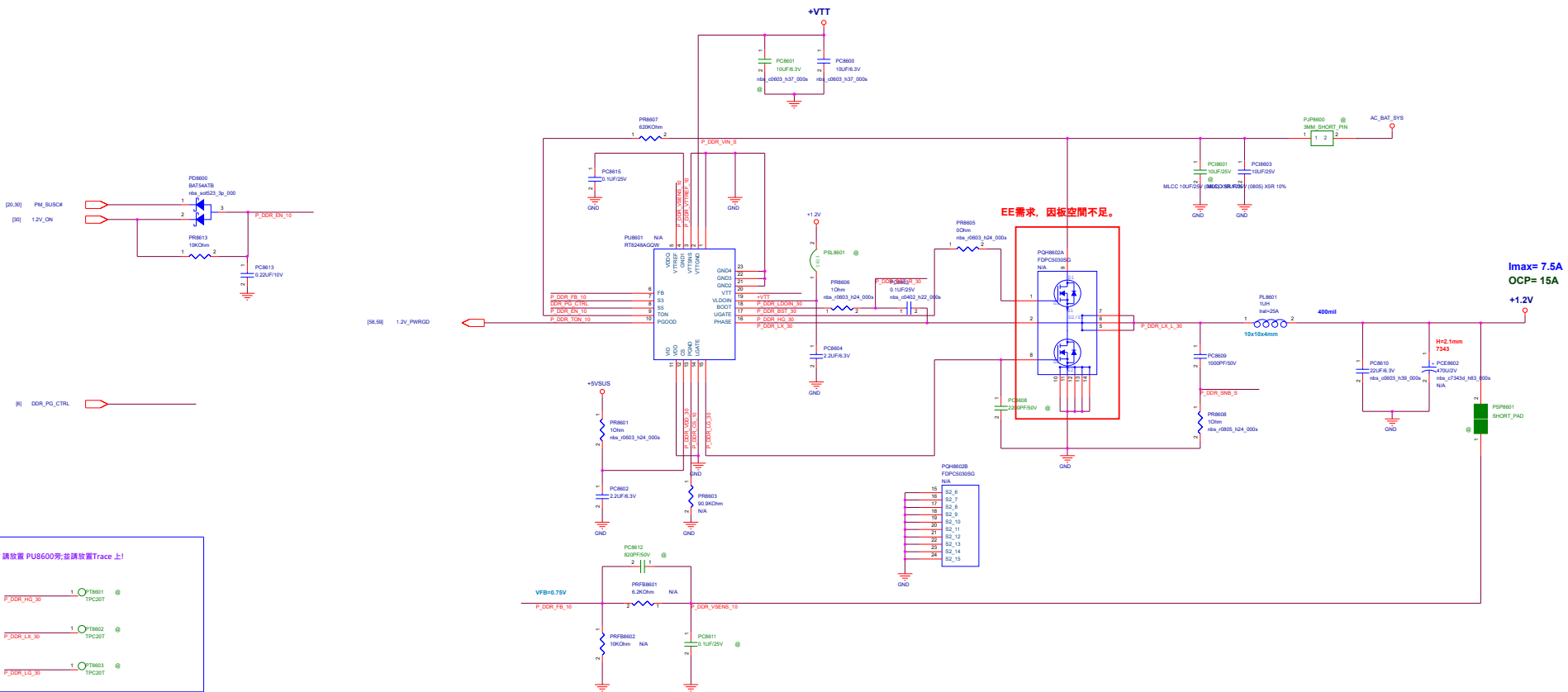
Note:

1. Design may alternatively use two 0201W 0.47 μ F X6S for each 0201W 1 μ F.

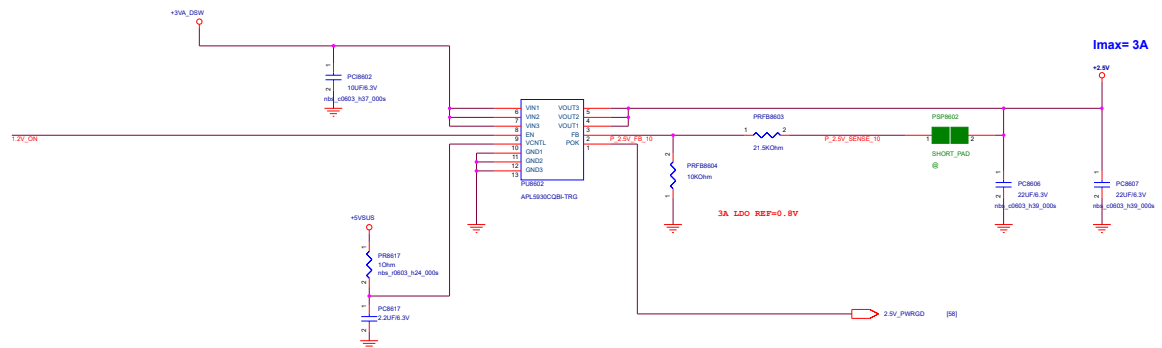
1V8_AON Supply Rail						
GB4C-128, GB4D-128	0.1 μ F	X7R	0402	0	2	Under GPU
	0.47 μ F ¹	X6S	0201W	4	0	Under GPU
	1.0 μ F ¹	X6S	0402 or 0201W	0	1	Near GPU
	0.47 μ F ¹	X6S	0201W	6	0	Near GPU
	4.7 μ F	X6S	0603	3	1	Near GPU



+1.2V / +VTT / +2.5V[For Memory]



PT860* 請放置 PU8600旁,並請放置Trace上!

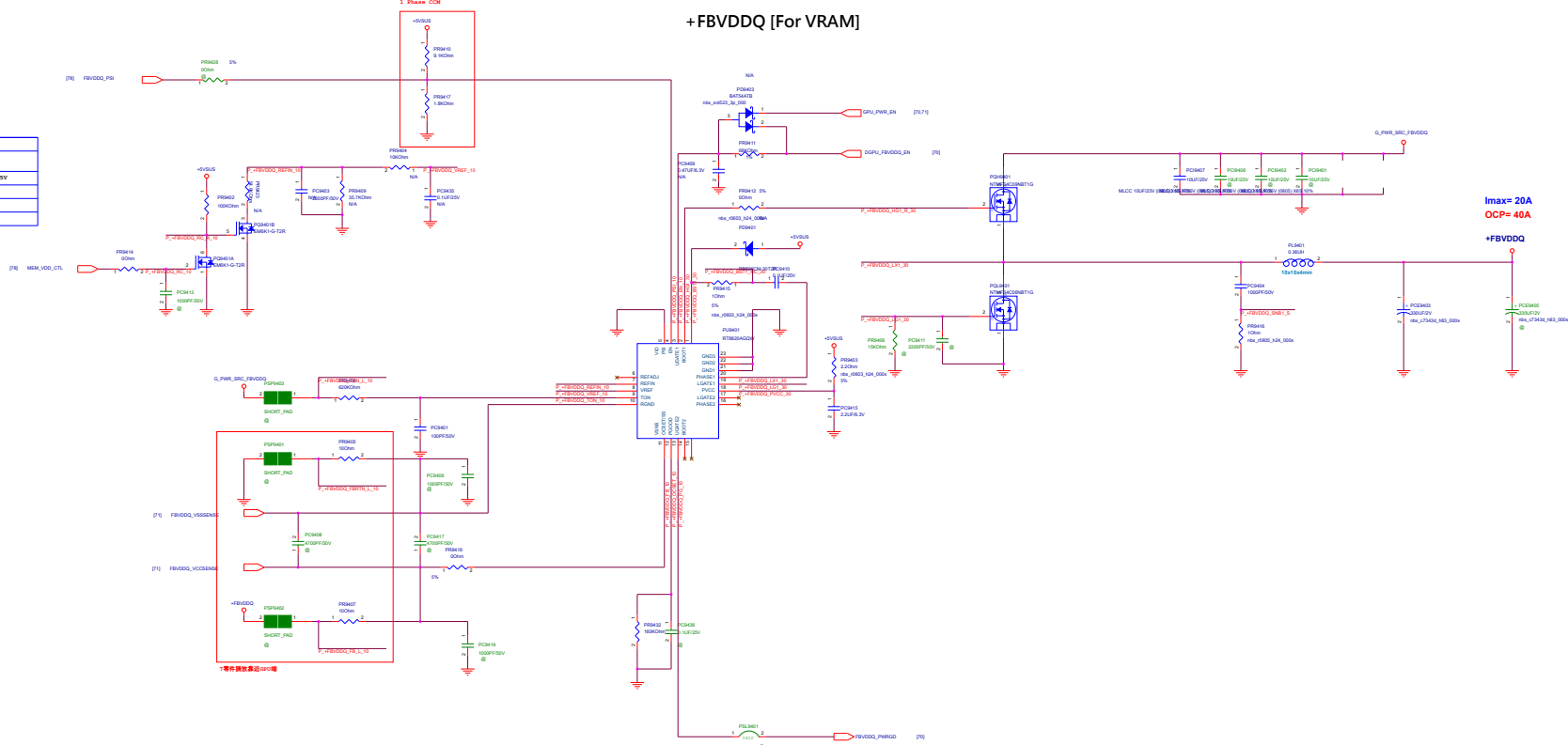


Imax= 3A

<Data Design>

Project Name		Rev
ASUS G711GW		R1.0
Title : PW_+1.2V/+VTT/+2.5V		
Size	Dept. : NB Power team	Engineer: Neil
Date: Tuesday, March 19, 2019	Sheet	88 of 103

DVS Setting		
MEM_VDD_CTL	R	L
Voltage	1.5V	1.35V
P9404	1.000u	
P9409	35.700u	
P9423	54.900u	



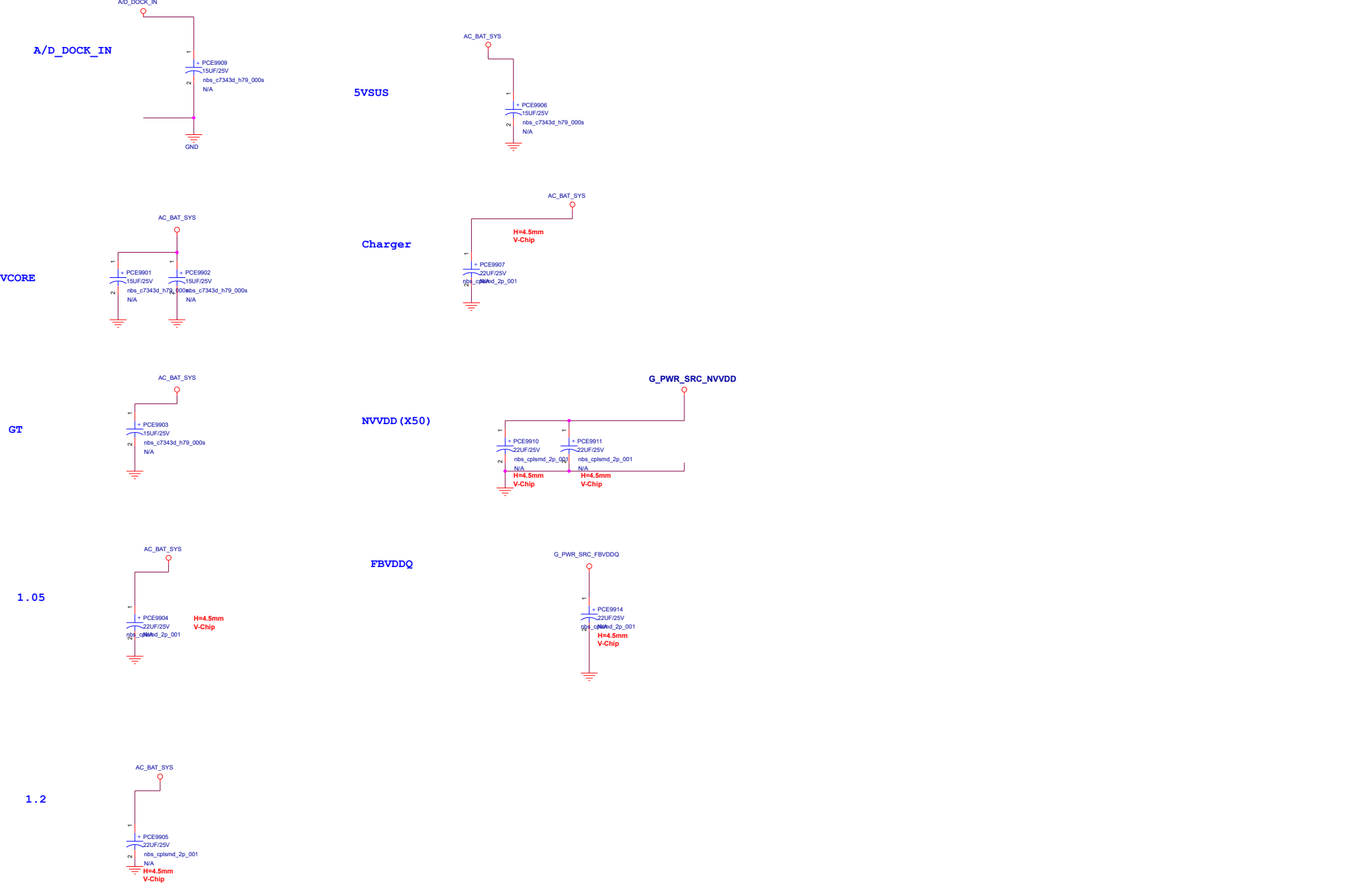
PT9407 請放置 P9401旁,並請放置Trace 上!

P9401 1 PT9401
NE_TPC20T


P9402 1 PT9402
NE_TPC20T

P9403 1 PT9403
NE_TPC20T

P9404 1 PT9404
NE_TPC20T



</variant Name>

		Project Name		Rev
		GM531GX		R1.0
Title : PW_Input CAP				
Size	Dept.: Power Team		Engineer: Joe	
Custom				
Date:	Tuesday, March 19, 2019	Sheet	99	of 102

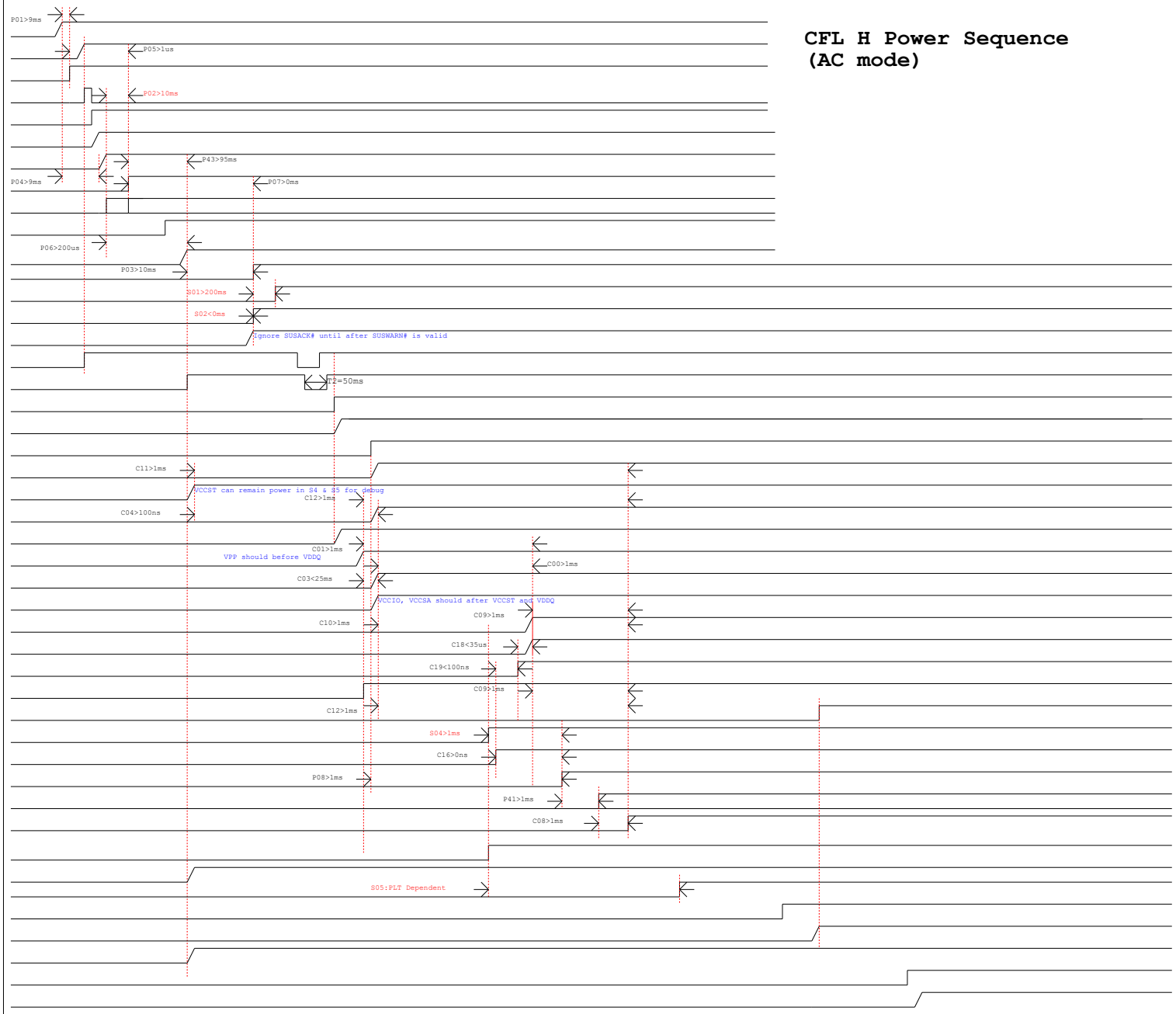
AC-IN Mode

C:CPU
 P:PCH
 S:PLT
 Power
 Signal

(+RTCBAT)+3VA_RTC
 (AC_BAT_SYS)+3VA/+5VA
 (+3VA_RTC)RTCRST#(PCH)
 (Power)AC_IN_OC#(EC)
 (EC)PS_ON(+3VA_EC)
 (PS_ON)+3VA_EC(EC)
 (3VADSW_ON)+3VA_DSW(3VA_DSW_PWRGD)
 (EC)DPWROK_EC(PCH)
 (+3VA_DSW)PM_BATLOW#(PCH)
 (PCH)PM_SLP_SUS#(EC)
 (VSUS_ON)+1.0VSUS_VCCPRIM(1.0VSUS_PWRGD)
 (EC)PM_RSMRST#_PCH(PCH)
 (PCH)SUSWARN#(EC)
 (EC)ME_AC_PRESENT_PCH(PCH)
 (EC)PCH_SUSACK#(PCH)
 (PWR_Switch)PWR_SW#(EC)
 (EC)PM_PWRBTN#(PCH)
 (EC)SUSC_EC#(Power)
 (SUSC_EC#)+12V/+5V/+3V
 (EC)SUSB_EC#(Power)
 (SUSB_EC#)+12VS/+5VS/+3VS
 (SUSB_EC#)+1.0V_VCCST,VCCPLL
 (SUSB_EC#)+VCCIO,(+12VS)+VCCSTG
 (1.2V_ON)+2.5V(2.5V_PWRGD)
 (1.2V_ON)+VDDQ_CPU(1.2V_PWRGD)
 (+12VS)+VCCPLL_OC
 (SUSB_EC#)+VCCIO(VCCIO_PWRGD)
 (ALL_SYSTEM_PWRGD)+VCCSA(IMVP8_PWRGD)
 (DDR_VTT_CTRL)+0.6V
 (CPU)DDR_VTT_CTRL(Power)
 (Power)1.2V_PWRGD(AND)
 (Power)IMVP8_PWRGD
 (AND)ALL_SYSTEM_PWRGD(CPU/PCH/EC/Power)
 (ALL_SYSTEM_PWRGD)VCCST_PWRGD_CPU(CPU)
 (EC)PM_PWROK_PCH(PCH)
 (PCH)CLK_PCH_BCLK(CPU)
 (PCH)H_CPUPWRGD(CPU)
 (CPU)P_SVID_DATA_X2(Power)
 (EC)PM_SYSPWROK_PCH(PCH)
 (PCH)PLT_RST#(CPU/EC/Device)
 (P_IMVP8_DRVON)+VCCCORE(IMVP8_PWRGD)
 (CPU)H_THERMTRIP#(PCH)
 (PCH)DDR4_DRAMRST#(Memory)

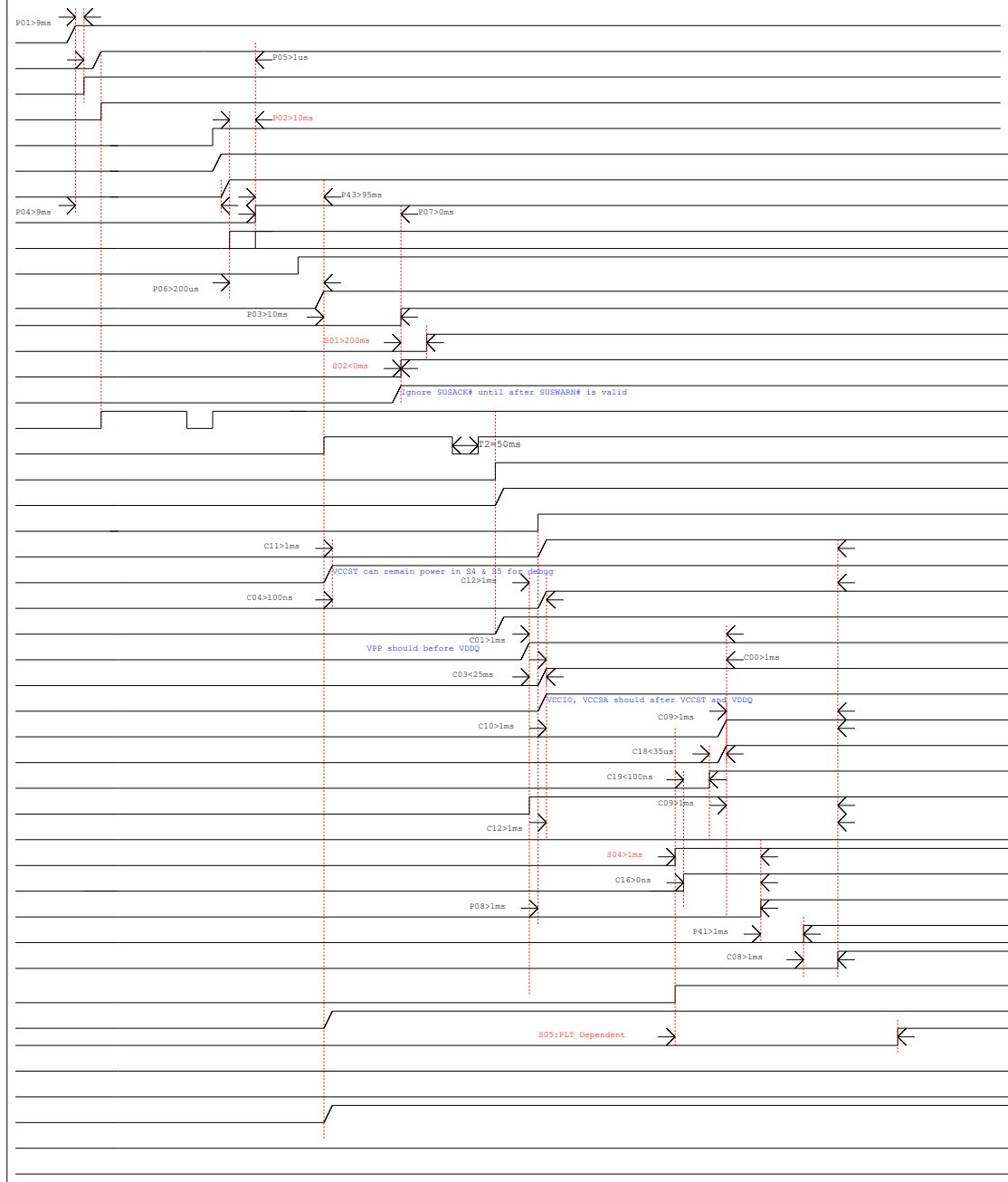
+VCCGT

CFL H Power Sequence (AC mode)



DC-IN Mode

C:CPU (+RTCBAT)+3VA_RTC
P:PCH (AC_BAT_SYS)+3VA/+5VA
S:PLT (+3VA_RTC) RTCRST# (PCH)
Power (Power) AC_IN_OC# (EC)
Signal (EC) PS_ON (+3VA_EC)
(PS_ON)+3VA_EC (EC)
(3VADSW_ON)+3VA_DSW (3VA_DSW_PWRGD)
(EC) DPWROK_EC (PCH)
(+3VA_DSW) PM_BATLOW# (PCH)
(PCH) PM_SLP_SUS# (EC)
(VSUS_ON)+1.0VSUS_VCCPRIM (1.0VSUS_PWRGD)
(EC) PM_RSMRST#_PCH (PCH)
(PCH) SUSWARN# (EC)
(EC) ME_AC_PRESENT_PCH (PCH)
(EC) PCH_SUSACK# (PCH)
(PWR_Switch) PWR_SW# (EC)
(EC) PM_PWRBTN# (PCH)
(EC) SUSC_EC# (Power)
(SUSC_EC#)+12V/+5V/+3V
(EC) SUSB_EC# (Power)
(SUSB_EC#)+12VS/+5VS/+3VS
(VSUS_ON)+1.0V_VCCST, VCCPLL (VCCST_PWRGD)
(+VCCIO)+VCCSTG
(1.2V_ON)+2.5V (2.5V_PWRGD)
(1.2V_ON)+VDDQ_CPU (1.2V_PWRGD)
(+12VS)+VCCPLL_OC
(SUSB_EC#)+VCCIO (VCCIO_PWRGD)
(ALL_SYSTEM_PWRGD)+VCCSA (IMVP8_PWRGD)
(DDR_VTT_CTRL)+0.6V
(CPU) DDR_VTT_CTRL (Power)
(Power) 1.2V_PWRGD (AND)
(Power) IMVP8_PWRGD
(AND) ALL_SYSTEM_PWRGD (CPU/PCH/EC/Power)
(ALL_SYSTEM_PWRGD) VCCST_PWRGD_CPU (CPU)
(EC) PM_PWROK_PCH (PCH)
(PCH) CLK_PCH_BCLK (CPU)
(PCH) H_CPU_PWRGD (CPU)
(ALL_SYSTEM_PWRGD) P_IMVP8_EN_10 (Power)
(CPU) P_SVID_DATA_X2 (Power)
(EC) PM_SYSPWROK_PCH (PCH)
(PCH) PLT_RST# (CPU/EC/Device)
(P_IMVP8_DRVON)+VCCCORE (IMVP8_PWRGD)
(CPU) H_THERMTRIP# (PCH)
(PCH) DDR4_DRAMRST# (Memory)
+VCCGT



CFL H Power Sequence
(DC mode)

G731GX SKU Table

Option	PCB	SRU	CPU	Power	DRAM	VRAM		
60MB0810-MB1030	R2.0	GR501VXK SRU1	/I7-7700HQ	/230W	8G_Rylix	VR0_Samsung		
60MB0810-MB2000	R2.0	GR501VXK SRU2	/I5-7300HQ	/230W	8G_Rylix	VR0_Samsung		

1. CPU: INT I7-7700HQ 2.8G/6M SR32Q BGA 01001-01380600
CPU: INT I5-7300HQ 2.5G/6M SR32S BGA 01001-01380500

2. dGPU: nVidia W7E-Q2-A1 FCBGA2152 02004-00480500

OPTION 0007041 101 PROXIMA 000000

4. EC: ITE IT8995VQ-128/DX --06037-00050800

5. onboard memory
8G_Rylix 03012-00030400

9. Card Reader: AM6435--02G630002400 (Page42)

10. USB Charger IC: (Page52) Sillego S1G55584VTR -- 06016-00040000
MAXIM MAX14566AERTX+ -- 06G016196011

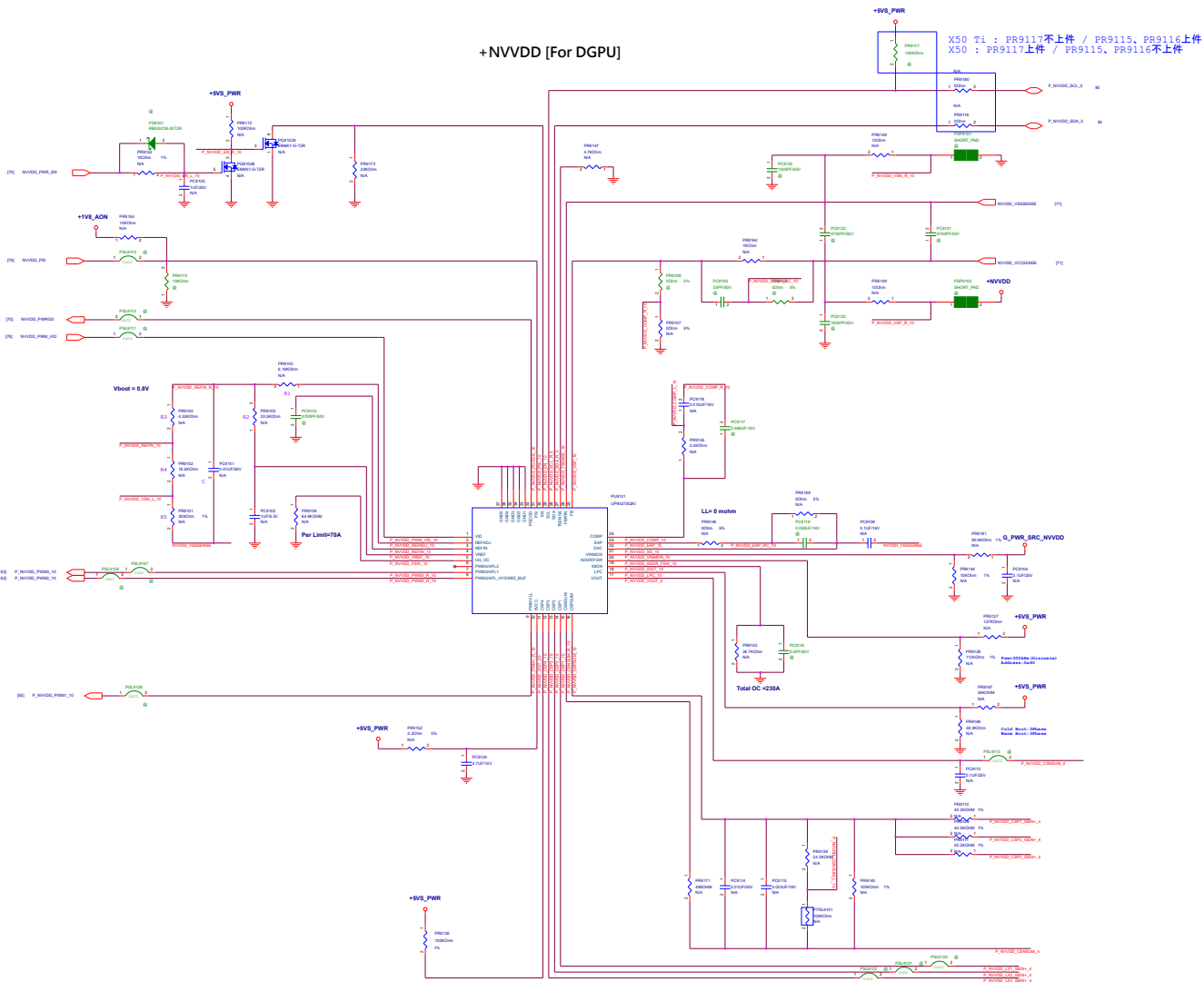
11. USB3.0 Repeater IC: (Page67)
Parade : P88710B -- 06053-00200000
Maxim : MAX14972CTG+ -- 06053-00030000

13. Audio Codec : 02043-00130000 (663-VA4)



請放靠近PU9101

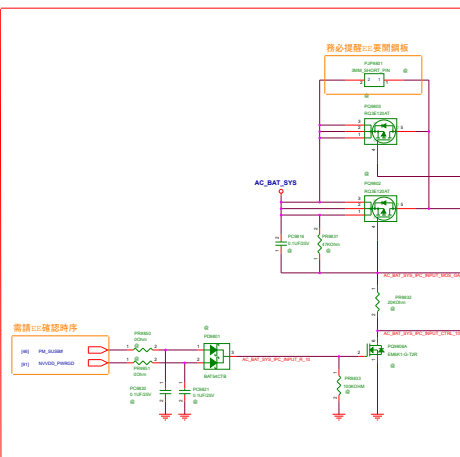
+NVVDD [For DGPU]



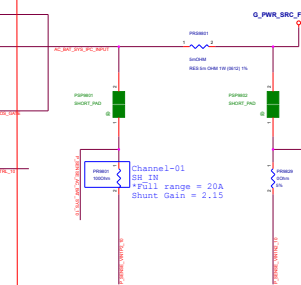
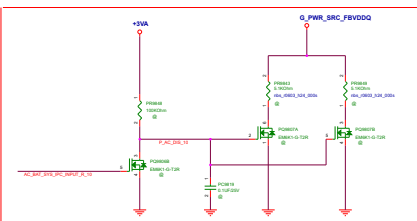
Client Name

Project Name
Title : PWR_NVVDD (2)

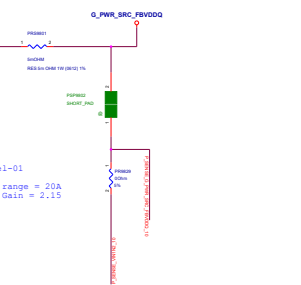
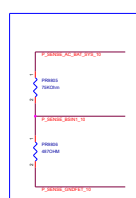
Rev	Rev	Rev
1.0	1.0	1.0



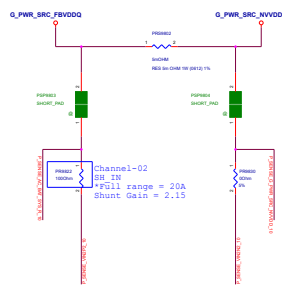
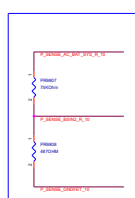
AC_BAT_SYS Discharge線路
T-Discharge : 0.626s (Worst case 10 Phase)



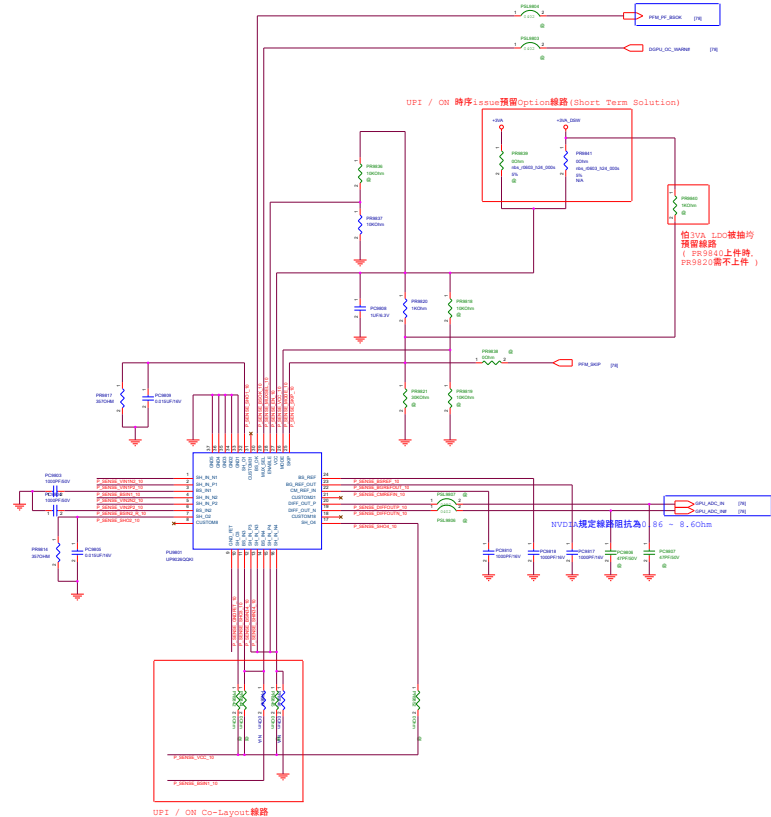
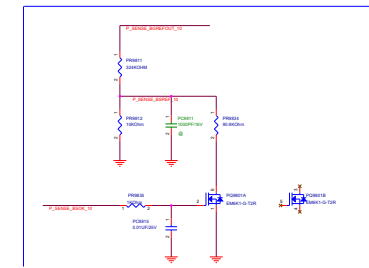
Channel-01
RS1 : ON
*Full range = 19V
Bus Gain = 6.4514m



Channel-02
RS1 : ON
*Full range = 19V
Bus Gain = 6.4514m



CH REF SW
*6.0331V, 5.4514V (此值需小於19V, BAT電壓)



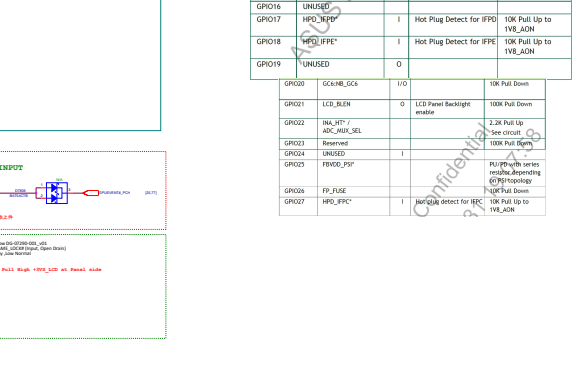
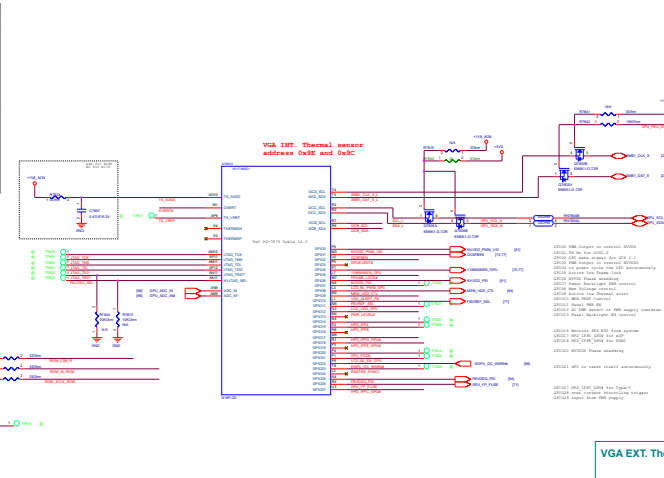
怕3VA Load被抽均預置線路
(PR9840上件時, PR9820需不上件)

N18E

150W+			115W ~ 130W			100W ~ 110W			75W ~ 90W			75W-					
UP9026PQKI (UPI)			NCP45491 (ON)			UP9026PQKI (UPI)			NCP45491 (ON)			UP9026PQKI (UPI)			NCP45491 (ON)		
PR9801	100k(10G212100014010)																
PR9817	127k (10G212127014010)	180k (10G212169014010)															
PR9822	100k(10G212100014010)																
PR9814	127k (10G212127014010)	180k (10G212169014010)															
PR9805	75k(10G212750214010)																
PR9806	487k (10G212487014010)	649k (10G212649014010)															
PR9807	75k(10G212750214010)																
PR9808	487k (10G212487014010)	649k (10G212649014010)															
PR9811	243k (10G212324314010)	243k (10G212243314010)															
PR9812	10k(10G212100214010)																
PR9834	90.9k(10G212909214010)																

N18P

75W-			150w+			115W ~ 130W			75W ~ 90W		
	UP9026PQKI (UPI)	NCP45491 (ON)		UP9026PQKI (UPI)	NCP45491 (ON)		UP9026PQKI (UPI)	NCP45491 (ON)		UP9026PQKI (UPI)	NCP45491 (ON)
PR9801	100k(10G212100014010)		PR9801	200k(10G212200014010)		PR9801	200k(10G212200014010)		PR9801	200k(10G212200014010)	
PR9817	75k(10G212357014010)	475k(10G212475014010)	PR9817	127k(10G212127014010)		PR9817	47k(10G212143014010)		PR9817	212k(10102-00571000)	
PR9822	100k(10G212100014010)		PR9822	200k(10G212200014010)		PR9822	200k(10G212200014010)		PR9822	200k(10G212200014010)	
PR9814	357k(10G212357014010)	475k(10G212475014010)	PR9814	127k(10G212127014010)		PR9814	47k(10G212143014010)		PR9814	212k(10102-00571000)	
PR9805	75k(10G212750214010)		PR9805	33k(10G212330214010)		PR9805	33k(10G212330214010)		PR9805	33k(10G212330214010)	
PR9806	487k(10G212487014010)	649k(10G212649014010)	PR9806	431k(10102-00581000)		PR9806	431k(10102-00581000)		PR9806	431k(10102-00581000)	
PR9807	75k(10G212750214010)		PR9807	33k(10G212330214010)		PR9807	33k(10G212330214010)		PR9807	33k(10G212330214010)	
PR9808	487k(10G212487014010)	649k(10G212649014010)	PR9808	431k(10102-00581000)		PR9808	431k(10102-00581000)		PR9808	431k(10102-00581000)	
PR9811	243k(10G212324314010)	243k(10G212243314010)	PR9811	324k(10G212324314010)		PR9811	324k(10G212324314010)		PR9811	324k(10G212324314010)	
PR9812	10k(10G212100214010)		PR9812	10k(10G212100214010)		PR9812	10k(10G212100214010)		PR9812	10k(10G212100214010)	
PR9834	90.9k(10G212909214010)		PR9834	90.9k(10G212909214010)		PR9834	90.9k(10G212909214010)		PR9834	90.9k(10G212909214010)	



			
Model Name: G731-OK			
Title: G731-OK			
Part	Serial	Customer	Service ID

GPO20	CCONB_CCA	1/0	10K Pull Down
GPO21	LCD_BLEN	0	LCD Panel Backlight enable 100K Pull Down
GPO22	INA_HCT/ ADC_MUX_SEL		2.2K Pull Up See circuit
GPO23	Reserved		100K Pull Down
GPO24	UNRESO	1	10K Pull Up
GPO25	TBD00_P5P		PU/PD with series resistor depending on P5P topology
GPO26	FS_FUSE		10K Pull Down
GPO27	HPD_FFC*	1	HPD detect for HPC 10K Pull Up to